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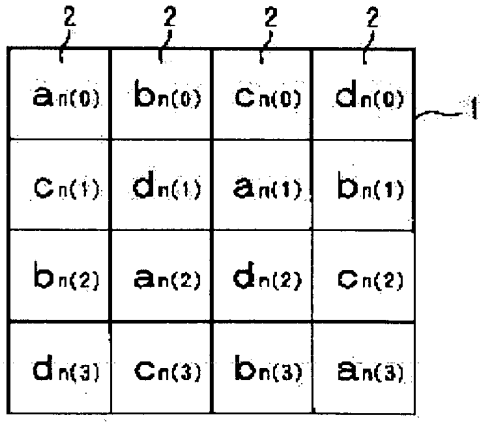
(54) USAGE OF MEMORY, TWO-DIMENSIONAL DATA ACCESS MEMORY, AND PROCESSOR

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a usage or the like of a memory capable of contributing to efficient SIMD(single instruction stream-multiple data stream) computing.
SOLUTION: In a virtual minimum two-dimensional memory space 1, a predetermined two-dimensional memory space arranged in the vertical and horizontal directions is assumed, and respective addresses of the virtual minimum two-dimensional memory space 1 are previously assigned to predetermined respective addresses of n physical memories addresses decided according to a relation with the virtual minimum two-dimensional memory space. In reading data, a reading address on the virtual minimum two-dimensional memory space 1 is designated while the vertical/horizontal reading direction of the data is designated by using the designated reading address as a reference, and according to the both designations, sequential data arranged in the vertical or horizontal direction on the virtual minimum two-dimensional memory space 1 are read from the addresses respectively corresponding to the n memories.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The predetermined two-dimensional room which arranged the predetermined virtual minimum two-dimensional room formed two-dimensional in the direction in every direction is assumed. Each address of said virtual minimum two-dimensional room is beforehand assigned to each predetermined address of n physical memory decided by relation with said virtual minimum two-dimensional room. When reading the data on said two-dimensional room While specifying the read-out address on said virtual minimum two-dimensional room If the longitudinal direction of data or the read-out direction of a lengthwise direction is specified on the basis of the specified read-out address Operation of the memory characterized by reading the continuation data on a par with the longitudinal direction or lengthwise direction on said virtual minimum two-dimensional room from the address with which said each n memory corresponds according to the assignment of both, respectively.
[Claim 2] furthermore, when writing in data on said two-dimensional room While specifying the write-in address on said virtual minimum two-dimensional room If the longitudinal direction of data or the write-in direction of a lengthwise direction is specified on the basis of the specified write-in address Operation of the memory according to claim 1 characterized by writing the continuation data which should be continuously written in the longitudinal direction or lengthwise direction on said virtual minimum two-dimensional room in the address with which said each n memory corresponds according to the assignment of both, respectively.
[Claim 3] The predetermined two-dimensional room which arranged the predetermined virtual minimum two-dimensional room formed two-dimensional in the direction in every direction is assumed. Each address of said virtual minimum two-dimensional room is beforehand assigned to each predetermined address of n physical memory decided by relation with said virtual minimum two-dimensional room. When reading the data on said two-dimensional room While specifying the read-out address on said virtual minimum two-dimensional room If the predetermined read-out pattern of data is specified on the basis of the specified read-out address Operation of the memory characterized by reading the predetermined data on said virtual minimum two-dimensional room from the address with which said each n memory corresponds according to the assignment of both, respectively.
[Claim 4] When memorizing some reference data in motion vector presumption of a dynamic image in said two-dimensional room and reading the data on said two-dimensional room Furthermore, if the predetermined data read-out approach in the case of motion vector presumption is specified It responds to the predetermined read-out pattern and said data read-out approach of said read-out address, the longitudinal direction of data according to claim 1, the read-out direction of a lengthwise direction, or data according to claim 3. In the virtual minimum two-dimensional room which read-out of data completed on the occasion of motion vector presumption When data are referred to ranging over the periphery of sequential writing and said two-dimensional room, consecutive predetermined reference data Operation of the memory according to claim 1 or 3 characterized by correcting the read-out address of the data concerned to the predetermined address of the virtual minimum two-dimensional room where consecutive predetermined reference data were written in, and reading it.
[Claim 5] When memorizing some reference data in motion vector presumption of a dynamic image in said two-dimensional room and reading the data on said two-dimensional room Furthermore, if the predetermined data read-out approach in the case of motion vector presumption is specified It responds to the predetermined read-out pattern and said data read-out approach of said read-out address, the longitudinal direction of data according to claim 1, the read-out direction of a lengthwise direction, or data according to claim 3. When data are referred to ranging over the periphery of the said reference data's

existence range Operation of the memory according to claim 1 or 3 characterized by correcting the read-out address of the data which are not contained in the said reference data's existence range to the address of the predetermined data located in the periphery of the said reference data's existence range, and reading it.

[Claim 6] While assuming the two-dimensional room which arranged the predetermined virtual minimum two-dimensional room formed two-dimensional in the direction in every direction n memory by which each address of said virtual minimum two-dimensional room is beforehand assigned to each under the fixed regulation, In the case of read-out of data, the access location on said virtual minimum two-dimensional room is pinpointed. According to the read-out access mode which specifies the direction or pattern which reads data from this pinpointed access location, each read-out data from said n memory is rearranged. The read-out data control section which outputs each of this rearranged read-out data to a package, At the time of assignment of the read-out address, it responds to said assignment read-out access mode and said specific access location. Or in straddling said virtual minimum two-dimensional room where the space to access adjoins, it responds to said assignment read-out access mode. Two-dimensional data access memory characterized by having the read-out address control section which corrects said assignment read-out address to the predetermined address, and is outputted to said n memory.

[Claim 7] The access location on said virtual minimum two-dimensional room where said read-out data control section is specified according to assignment of the read-out address in the case of read-out of data, It is prepared corresponding to the data controller which outputs the selection signal which chooses the read-out data of said n memory according to assignment of said read-out access mode, and said n memory. It has n selectors which choose each read-out data from said n memory based on the selection signal from said data controller, and are outputted to coincidence. Said read-out address control section While outputting the address translation signal which changes into a predetermined value said read-out address which is equivalent to the address by the side of the low order of each of said memory according to said read-out access mode and said read-out address at the time of assignment of the read-out address In straddling said virtual minimum two-dimensional room where the space to access adjoins The address controller which outputs the amendment signal which amends said read-out address which is equivalent to the address by the side of the high order of each of said memory according to said read-out access mode, While being prepared corresponding to said n memory, changing said read-out address into a predetermined value with the address translation signal from said address controller and outputting to said each memory Two-dimensional data access memory according to claim 6 characterized by having the n address amendment sections which amend said read-out address with the amendment signal from said address controller, and are outputted to said each memory.

[Claim 8] Said read-out data control section is added to said assignment read-out access mode and said specific access location. According to the option mode in which the data read-out approach in motion vector presumption is specified, each read-out data from said n memory is rearranged. Each of this rearranged read-out data is outputted to a package. Said read-out address control section At the time of assignment of the read-out address, it responds to said assignment read-out access mode and said specific access location. Or in straddling said virtual minimum two-dimensional room where the space to access adjoins, it responds to said assignment read-out access mode. The read-out address control section which corrects said assignment read-out address to the predetermined address according to said read-out access mode and said option mode, and is outputted to said n memory when the space furthermore accessed straddles the periphery of said two-dimensional room, Two-dimensional data access memory according to claim 6 characterized by preparation ******.

[Claim 9] The access location on said virtual minimum two-dimensional room where said read-out data control section is specified according to assignment of the read-out address in the case of read-out of data, The data controller which outputs the selection signal which chooses the read-out data of said n memory according to assignment of said read-out access mode, and assignment in said option mode, It has n selectors which are prepared corresponding to said n memory, choose each read-out data from said n memory based on the selection signal from said data controller, and are outputted to coincidence. Said read-out address control section responds to said read-out access mode and said read-out address at the time of assignment of the read-out address. While outputting the address translation signal which changes said read-out address equivalent to the address by the side of the low order of each of said memory into a predetermined value In straddling said virtual minimum two-dimensional room where the space to access adjoins The amendment signal which amends said read-out address which is equivalent to the address by the side of the high order of each of said memory according to said read-out access mode is outputted. The address controller which outputs the signal which amends the address by the side of the high order of

each of said memory according to said read-out access mode and said option mode when the space furthermore accessed straddles the periphery of said two-dimensional room, While being prepared corresponding to said n memory, changing said read-out address into a predetermined value with the address translation signal from said address controller and outputting to said each memory Two-dimensional data access memory according to claim 8 characterized by having the n address amendment sections which amend said read-out address with the amendment signal from said address controller, and are outputted to said each memory.

[Claim 10] The access location on said virtual minimum two-dimensional room where said read-out data control section is specified according to assignment of the read-out address in the case of read-out of data, The data controller which outputs the selection signal which chooses the read-out data of said n memory according to assignment of said read-out access mode, and assignment in said option mode, It has n selectors which are prepared corresponding to said n memory, choose each read-out data from said n memory based on the selection signal from said data controller, and are outputted to coincidence. Said read-out address control section responds to said read-out access mode and said read-out address at the time of assignment of the read-out address. While outputting the address translation signal which changes said read-out address equivalent to the address by the side of the low order of each of said memory into a predetermined value In straddling said virtual minimum two-dimensional room where the space to access adjoins The amendment signal which amends said read-out address which is equivalent to the address by the side of the high order of each of said memory according to said read-out access mode is outputted. The address controller which outputs the signal which amends the address by the side of the high order of each of said memory, and low order according to said read-out access mode and said option mode when the space furthermore accessed straddles the periphery of the data's which said two-dimensional room's has memorized existence range, While being prepared corresponding to said n memory, changing said read-out address into a predetermined value with the address translation signal from said address controller and outputting to said each memory Two-dimensional data access memory according to claim 8 characterized by having the n address amendment sections which amend said read-out address with the amendment signal from said address controller, and are outputted to said each memory.

[Claim 11] In the case of the writing of data, the access location on said virtual minimum two-dimensional room is pinpointed. According to the write-in access mode which specifies the direction which writes in data, each write-in data to said n memory is rearranged from this pinpointed access location. The write-in data control section which supplies each of this write-in rearranged data to a package at said n memory, At the time of assignment of the write-in address, it responds to said assignment write-in access mode and said specific access location. Or in straddling said virtual minimum two-dimensional room where the space to access adjoins, it responds to said assignment write-in access mode. Two-dimensional data access memory according to claim 6 or 7 characterized by having further the write-in address control section which corrects the predetermined address and outputs said assignment write-in address to said n memory.

[Claim 12] The access location on said virtual minimum two-dimensional room where said write-in data control section is specified according to assignment of the write-in address in the case of the writing of data, The data controller which outputs the selection signal which chooses the write-in data of said n memory according to assignment of said write-in access mode, It has n selectors which are prepared corresponding to said n memory, choose each write-in data to said n memory based on the selection signal from said data controller, and are supplied to coincidence at each of that memory. A write-in address control section responds to said write-in access mode and said write-in address at the time of assignment of the write-in address. While outputting the address translation signal which changes said write-in address equivalent to the address by the side of the low order of each of said memory into a predetermined value In straddling said virtual minimum two-dimensional room where the space to access adjoins The address controller which outputs the amendment signal which amends said write-in address which is equivalent to the address by the side of the high order of each of said memory according to said write-in access mode, While being prepared corresponding to said n memory, changing said write-in address into a predetermined value with the address translation signal from said address controller and outputting to said each memory Two-dimensional data access memory according to claim 11 characterized by having the n address amendment sections which amend said write-in address with the amendment signal from said address controller, and are outputted to said each memory.

[Claim 13] The processing unit characterized by having the SIMD mold processor which specifies said access mode, reads predetermined data from said two-dimensional data access memory, and performs SIMD processing while specifying said address of said two-dimensional data access memory as either

claim 6 or claim 7 and claim 11 or claim 12 according to the two-dimensional data access memory of a publication, and a predetermined operation.
[Claim 14] Said predetermined operation is a processing unit according to claim 13 characterized by being a two-dimensional discrete cosine transform.
[Claim 15] The processing unit characterized by having two-dimensional data access memory according to claim 8 to 10 and the SIMD mold processor which specifies said access mode and said option mode, reads predetermined data from said two-dimensional data access memory, and performs SIMD processing while specifying said address of said two-dimensional data access memory according to a predetermined operation.
[Claim 16] Said predetermined operation is a processing unit according to claim 15 characterized by being data processing concerning motion vector presumption of a dynamic image.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the processing unit which can perform a SIMD operation efficiently using the two-dimensional data access memory which instrumentated the operation of the memory which an efficient SIMD (Single Instruction stream Multiple Data stream) operation becomes realizable, and the operation of this memory, and its two-dimensional data access memory.
[0002]
[Description of the Prior Art] A SIMD operation is a method which has two or more processors and processes two or more data with the same instruction. For this reason, it is very efficient, when taking out a part of continuous partial sequence and performing parallel operation from the 1-dimensional data stream memorized by memory generally.
[0003] However, the data used as the candidate for an operation continue on memory, and are not memorized, or the processing for preparing the data for parallel operation and the processing for arranging a parallel operation result in the predetermined location of memory are needed to distribute and arrange the result of an operation in the predetermined location on memory. For this reason, there is un-arranging [that the goodness of original parallel processing is checked].
[0004]
[Problem(s) to be Solved by the Invention] By the way, invention of a publication is known by JP,2000-69478,A as a technique which can accelerate two-dimensional discrete cosine transform processing by SIMD processing. This invention is rearranged into the sequence suitable for performing a butterfly session [in / for the image data arranged in order of a scan / a conversion coding operation] by SIMD processing, memorizes this rearrangement result in memory, and carries out the two-dimensional discrete cosine transform of the image data memorized by that memory.
[0005] However, in the actuation which rearranges image data is needed for the above-mentioned official report by invention of a publication and realizing by hardware, the circuit of the part concerning the actuation to rearrange is needed, it is possible above un-arranging [that a circuit scale becomes large], and it is also un-arranging [that power consumption becomes large by the memory access by rearrangement actuation].
[0006] Then, the 1st purpose of this invention is to offer the operation of the memory which can contribute to the increase in efficiency of a SIMD operation in view of the above-mentioned point. Moreover, the 2nd purpose of this invention enables it to access the continuation data or discontinuity data located in a line with the longitudinal direction and the lengthwise direction from the specified location on two-dimensional room, and is to offer the two-dimensional data access memory which can realize an efficient SIMD operation.
[0007] Furthermore, the 3rd purpose of this invention is by using two-dimensional data access memory to offer the processing unit which can perform a SIMD operation efficiently.
[0008]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem and to attain the 1st purpose of this invention, invention according to claim 1 to 5 was constituted as follows. Invention according to claim 1 namely, the predetermined virtual minimum two-dimensional room formed two-dimensional The predetermined two-dimensional room arranged in the direction in every direction is assumed. Each address of said virtual minimum two-dimensional room When assigning beforehand each predetermined address of n physical memory decided by relation with said virtual minimum two-dimensional room and reading the data on said two-dimensional room While specifying the read-out

address on said virtual minimum two-dimensional room If the longitudinal direction of data or the read-out direction of a lengthwise direction is specified on the basis of the specified read-out address It is characterized by reading the continuation data on a par with the longitudinal direction or lengthwise direction on said virtual minimum two-dimensional room from the address with which said each n memory corresponds according to the assignment of both, respectively.
[0009] moreover, in the operation of memory according to claim 1, further, when writing in data on said two-dimensional room, invention according to claim 2 While specifying the write-in address on said virtual minimum two-dimensional room If the longitudinal direction of data or the write-in direction of a lengthwise direction is specified on the basis of the specified write-in address It is characterized by writing the continuation data which should be continuously written in the longitudinal direction or lengthwise direction on said virtual minimum two-dimensional room in the address with which said each n memory corresponds according to the assignment of both, respectively.
[0010] Invention according to claim 3 moreover, the predetermined virtual minimum two-dimensional room formed two-dimensional The predetermined two-dimensional room arranged in the direction in every direction is assumed. Each address of said virtual minimum two-dimensional room When assigning beforehand each predetermined address of n physical memory decided by relation with said virtual minimum two-dimensional room and reading the data on said two-dimensional room While specifying the read-out address on said virtual minimum two-dimensional room If the predetermined read-out pattern (for example, pattern in the alternate mode shown in drawing 19 or drawing 20) of data is specified on the basis of the specified read-out address It is characterized by reading the predetermined data on said virtual minimum two-dimensional room from the address with which said each n memory corresponds according to the assignment of both, respectively.
[0011] Moreover, invention according to claim 4 is set to the operation of memory according to claim 1 or 3. Reference data [in / in said two-dimensional room / motion vector presumption of a dynamic image] When memorizing a part of (for example, reference frame of drawing 31) and reading the data on said two-dimensional room Furthermore, if the predetermined data read-out approach in the case of motion vector presumption (for example, circular mode in the 2nd operation gestalt) is specified It responds to the predetermined read-out pattern and said data read-out approach of said read-out address, the longitudinal direction of data according to claim 1, the read-out direction of a lengthwise direction, or data according to claim 3. In the virtual minimum two-dimensional room which read-out of data completed on the occasion of motion vector presumption When data are referred to ranging over the periphery (for example, boundary of the storage region of the two-dimensional room 3 of drawing 15) of sequential writing and said two-dimensional room, consecutive predetermined reference data It is characterized by correcting the read-out address of the data concerned to the predetermined address of the virtual minimum two-dimensional room where consecutive predetermined reference data were written in, and reading it.
[0012] Moreover, invention according to claim 5 is set to the operation of memory according to claim 1 or 3. When memorizing some reference data in motion vector presumption of a dynamic image in said two-dimensional room and reading the data on said two-dimensional room Furthermore, if the predetermined data read-out approach in the case of motion vector presumption (for example, padding mode in the 2nd operation gestalt) is specified It responds to the predetermined read-out pattern and said data read-out approach of said read-out address, the longitudinal direction of data according to claim 1, the read-out direction of a lengthwise direction, or data according to claim 3. When data are referred to ranging over the periphery (for example, image boundary of drawing 18) of the said reference data's existence range (for example, range where the data of the reference frame of drawing 18 exist) It is characterized by correcting the read-out address of the data which are not contained in the said reference data's existence range to the address of the predetermined data located in the periphery of the said reference data's existence range, and reading it.
[0013] According to invention according to claim 1 to 5 which consists of such a configuration, it can contribute to the increase in efficiency of a SIMD operation. Moreover, according to invention according to claim 3 to 5 which consists of such a configuration, it can contribute to the increase in efficiency of processing concerning motion vector presumption of a dynamic image. Moreover, in order to attain the 2nd purpose of this invention, each invention according to claim 6 to 12 was constituted as follows.
[0014] Namely, while invention according to claim 6 assumes the two-dimensional room which arranged the predetermined virtual minimum two-dimensional room formed two-dimensional in the direction in every direction n memory by which each address of said virtual minimum two-dimensional room is beforehand assigned to each under the fixed regulation, In the case of read-out of data, the access location on said virtual minimum two-dimensional room is pinpointed. According to the read-out access mode

which specifies the direction or pattern which reads data from this pinpointed access location, each read-out data from said n memory is rearranged. The read-out data control section which outputs each of this rearranged read-out data to a package, On schedule [of the read-out address], it responds to said assignment read-out access mode and said specific access location. Or in straddling said virtual minimum two-dimensional room where the space to access adjoins, it responds to said assignment read-out access mode. It is characterized by having the read-out address control section which corrects said assignment read-out address to the predetermined address, and is outputted to said n memory.

[0015] Invention according to claim 7 is set in two-dimensional data access memory according to claim 6. Moreover, said read-out data control section The access location on said virtual minimum two-dimensional room pinpointed according to assignment of the read-out address in the case of read-out of data, It is prepared corresponding to the data controller which outputs the selection signal which chooses the read-out data of said n memory according to assignment of said read-out access mode, and said n memory. It has n selectors which choose each read-out data from said n memory based on the selection signal from said data controller, and are outputted to coincidence. Said read-out address control section While outputting the address translation signal which changes into a predetermined value said read-out address which is equivalent to the address by the side of the low order of each of said memory according to said read-out access mode and said read-out address at the time of assignment of the read-out address In straddling said virtual minimum two-dimensional room where the space to access adjoins The address controller which outputs the amendment signal which amends said read-out address which is equivalent to the address by the side of the high order of each of said memory according to said read-out access mode, While being prepared corresponding to said n memory, changing said read-out address into a predetermined value with the address translation signal from said address controller and outputting to said each memory It is characterized by having the n address amendment sections which amend said read-out address with the amendment signal from said address controller, and are outputted to said each memory.

[0016] Invention according to claim 8 is set in two-dimensional data access memory according to claim 6. Moreover, said read-out data control section The option mode in which the data read-out approach in motion vector presumption is specified in addition to said assignment read-out access mode and said specific access location According to for example, the 2nd (circular mode or padding mode) in an operation gestalt, each read-out data from said n memory is rearranged. Each of this rearranged read-out data is outputted to a package. Said read-out address control section At the time of assignment of the read-out address, it responds to said assignment read-out access mode and said specific access location. Or in straddling said virtual minimum two-dimensional room where the space to access adjoins, it responds to said assignment read-out access mode. The space furthermore accessed is the periphery (for example) of said two-dimensional room. The read-out address control section which corrects said assignment read-out address to the predetermined address according to said read-out access mode and said option mode, and it outputs to said n memory in straddling the boundary of the storage region of the two-dimensional room 3 of drawing 15 , It is characterized by preparation ******.

[0017] Invention according to claim 9 is set in two-dimensional data access memory according to claim 8. Moreover, said read-out data control section The access location on said virtual minimum two-dimensional room pinpointed according to assignment of the read-out address in the case of read-out of data, The data controller which outputs the selection signal which chooses the read-out data of said n memory according to assignment of said read-out access mode, and assignment in said option mode (for example, circular mode of the 2nd operation gestalt), It has n selectors which are prepared corresponding to said n memory, choose each read-out data from said n memory based on the selection signal from said data controller, and are outputted to coincidence. Said read-out address control section responds to said read-out access mode and said read-out address at the time of assignment of the read-out address. While outputting the address translation signal which changes said read-out address equivalent to the address by the side of the low order of each of said memory into a predetermined value In straddling said virtual minimum two-dimensional room where the space to access adjoins The amendment signal which amends said read-out address which is equivalent to the address by the side of the high order of each of said memory according to said read-out access mode is outputted. The space furthermore accessed is the periphery (for example) of said two-dimensional room. The address controller which outputs the signal which amends the address by the side of the high order of each of said memory according to said read-out access mode and said option mode in straddling the boundary of the storage region of the two-dimensional room 3 of drawing 15 , While being prepared corresponding to said n memory, changing said read-out address into a predetermined value with the address translation signal from said address controller and outputting to said each memory It is characterized by having the n address amendment

sections which amend said read-out address with the amendment signal from said address controller, and are outputted to said each memory.
[0018] Invention according to claim 10 is set in two-dimensional data access memory according to claim 8. Moreover, said read-out data control section The access location on said virtual minimum two-dimensional room pinpointed according to assignment of the read-out address in the case of read-out of data, The data controller which outputs the selection signal which chooses the read-out data of said n memory according to assignment of said read-out access mode, and assignment in said option mode (for example, padding mode of the 2nd operation gestalt), It has n selectors which are prepared corresponding to said n memory, choose each read-out data from said n memory based on the selection signal from said data controller, and are outputted to coincidence. Said read-out address control section responds to said read-out access mode and said read-out address at the time of assignment of the read-out address. While outputting the address translation signal which changes said read-out address equivalent to the address by the side of the low order of each of said memory into a predetermined value In straddling said virtual minimum two-dimensional room where the space to access adjoins The amendment signal which amends said read-out address which is equivalent to the address by the side of the high order of each of said memory according to said read-out access mode is outputted. The address controller which outputs the signal which amends the address by the side of the high order of each of said memory, and low order according to said read-out access mode and said option mode when the space furthermore accessed straddles the periphery of the data's which said two-dimensional room's has memorized existence range, While being prepared corresponding to said n memory, changing said read-out address into a predetermined value with the address translation signal from said address controller and outputting to said each memory It is characterized by having the n address amendment sections which amend said read-out address with the amendment signal from said address controller, and are outputted to said each memory.
[0019] Furthermore, invention according to claim 11 is set in two-dimensional data access memory according to claim 6 or 7. In the case of the writing of data, the access location on said virtual minimum two-dimensional room is pinpointed. According to the write-in access mode which specifies the direction which writes in data, each write-in data to said n memory is rearranged from this pinpointed access location. The write-in data control section which supplies each of this write-in rearranged data to a package at said n memory, At the time of assignment of the write-in address, it responds to said assignment write-in access mode and said specific access location. Or in straddling said virtual minimum two-dimensional room where the space to access adjoins, it responds to said assignment write-in access mode. It is characterized by having further the write-in address control section which corrects the predetermined address and outputs said assignment write-in address to said n memory.
[0020] Invention according to claim 12 is set in two-dimensional data access memory according to claim 5. Moreover, said write-in data control section The access location on said virtual minimum two-dimensional room pinpointed according to assignment of the write-in address in the case of the writing of data, The data controller which outputs the selection signal which chooses the write-in data of said n memory according to assignment of said write-in access mode, It has n selectors which are prepared corresponding to said n memory, choose each write-in data to said n memory based on the selection signal from said data controller, and are supplied to coincidence at each of that memory. A write-in address control section responds to said write-in access mode and said write-in address at the time of assignment of the write-in address. While outputting the address translation signal which changes said write-in address equivalent to the address by the side of the low order of each of said memory into a predetermined value In straddling said virtual minimum two-dimensional room where the space to access adjoins The address controller which outputs the amendment signal which amends said write-in address which is equivalent to the address by the side of the high order of each of said memory according to said write-in access mode, While being prepared corresponding to said n memory, changing said write-in address into a predetermined value with the address translation signal from said address controller and outputting to said each memory It is characterized by having the n address amendment sections which amend said write-in address with the amendment signal from said address controller, and are outputted to said each memory.
[0021] Since the continuation data located in a line with the longitudinal direction or the lengthwise direction from the specified location on two-dimensional room can be read from each physical memory to coincidence according to invention according to claim 6 to 10 which consists of such a configuration, an efficient SIMD operation becomes realizable. Moreover, since it can write in physical each memory at coincidence so that the continuation data which was located in a line with the longitudinal direction from the specified location on two-dimensional room or the lengthwise direction according to claim 11 which

consists of the above configurations, and invention according to claim 12 can be read to coincidence upwards from physical each memory and data may be continuously located in a line with the longitudinal direction from the specified location on two-dimensional room, or a lengthwise direction, it becomes realizable [an efficient SIMD operation].
[0022] Moreover, according to invention according to claim 8 to 10 which consists of the above configurations, it can contribute to the increase in efficiency of processing concerning motion vector presumption of a dynamic image. Furthermore, in order to attain the 3rd purpose of this invention, invention according to claim 13 to 16 was constituted as follows. That is, invention according to claim 13 is characterized by having the SIMD mold processor which specifies said access mode, reads predetermined data from said two-dimensional data access memory, and performs SIMD processing while it specifies said address of said two-dimensional data access memory as either claim 6 or claim 7 and claim 11 or claim 12 according to the two-dimensional data access memory of a publication, and a predetermined operation.
[0023] Moreover, invention according to claim 14 is characterized by said predetermined operation being a two-dimensional discrete cosine transform in a processing unit according to claim 13. Furthermore, invention according to claim 15 is characterized by having two-dimensional data access memory according to claim 8 to 10 and the SIMD mold processor which specifies said access mode and said option mode, reads predetermined data from said two-dimensional data access memory, and performs SIMD processing while specifying said address of said two-dimensional data access memory according to a predetermined operation.
[0024] Moreover, invention according to claim 16 is characterized by said predetermined operation being data processing concerning motion vector presumption of a dynamic image in a processing unit according to claim 15. According to claim 13 which consists of such a configuration, and invention according to claim 16, since two-dimensional data access memory is used, a SIMD operation can be performed efficiently.
[0025]
[Embodiment of the Invention] (Gestalt of the 1st operation) The operation gestalt of the operation of the memory of this invention is hereafter explained with reference to a drawing. By the operation of the memory concerning this operation gestalt, since the virtual minimum two-dimensional room 1 as shown in drawing 1 is appointed, this is explained first.
[0026] As the virtual minimum two-dimensional room 1 is shown in drawing 1 , a total of every four storage elements [16] 2 of the imagination of a smallest unit in which 1 byte (8 bits) of storage is possible is arranged in a lengthwise direction and a longitudinal direction, respectively. Therefore, it is constituted from 4 BAITORA [4 bytes of] = 16 bytes by this example. In addition, 8= 64 bytes of 8 RA etc. is possible for the magnitude of the virtual minimum two-dimensional room 1 in addition to the above-mentioned 16 bytes.
[0027] Physically, it is beforehand divided into four physical memory 4A-4C, and such virtual minimum two-dimensional room 1 is mapped, as shown in drawing 2 . That is, the one virtual minimum two-dimensional room 1 is equivalent to 4 bytes of continuation field which begins from the same address of four physical memory 4A-4C. each address an of the virtual minimum two-dimensional room 1 specifically shown in drawing 1 (0), bn (0), cn (0), and dn (0) -- the predetermined address an of each memory 4A-4D which shows ... to drawing 2 (0), bn (0), cn (0), and dn (0) -- it is beforehand assigned to ..., respectively.
[0028] Moreover, by the operation of the memory concerning this operation gestalt, since the two-dimensional room 3 as shown in drawing 3 is assumed, this is explained. The two-dimensional room 3 arranges the virtual minimum two-dimensional room 1 in the shape of a tile to a longitudinal direction and a lengthwise direction, as shown in drawing 3 . In this two-dimensional room 3, if the number which arranges the virtual minimum two-dimensional room 1 in a longitudinal direction is the exponentiation of 2, it can be set as arbitration, and it is taken as n bytes of 16 BAITORA in the example shown in drawing 3 .
[0029] Next, the operation of the memory concerning this operation gestalt is explained with reference to drawing 1 - drawing 4 . First, the two-dimensional room 3 which arranged the virtual minimum two-dimensional room 1 as shown in drawing 1 in the shape of a tile in the direction in every direction as shown in drawing 3 is assumed. On the other hand, each address of the virtual minimum two-dimensional room 1 is beforehand assigned to each four physical predetermined address of Memory 4A-4D decided by relation with the magnitude of the virtual minimum two-dimensional room 1, and is set to it (refer to drawing 1 and drawing 2). (matching)

[0030] Next, the read-out actuation from the memory 4A-4D at the time of reading the continuous data from the address of the arbitration on the virtual minimum two-dimensional room 1 is explained. In this case, while specifying the read-out address of that arbitration, the read-out access mode which specifies the read-out direction of data is specified. There are the line writing direction access mode, the direction access mode of a train, and the 2 steps of line writing direction access mode as this read-out access mode.
[0031] As shown in M1 of drawing 4 , the line writing direction access mode reads data from the read-out address of the arbitration on the virtual minimum two-dimensional room 1 to a line writing direction (longitudinal direction) like 8 BITTORA 4, 16 BITTORA 2, or 32 BITTORA 1, and can consider 16 kinds of accesses. As shown in M2 of drawing 4 , the direction access mode of a train reads data in the direction of a train (lengthwise direction) from the read-out address of the arbitration on the virtual minimum two-dimensional room 1 like 8 BITTORA 4, and can consider 16 kinds of accesses.
[0032] As shown in M3 of drawing 4 , the 2 steps of line writing direction access mode is crossed to two steps of line writing directions from the address of the arbitration on the virtual minimum two-dimensional room 1, reads data like 16 BITTORA 2, and can consider eight kinds of accesses. In this mode, the line writing direction is limited only per 2 bytes. Thus, if the read-out address of the arbitration on the virtual minimum two-dimensional room 1 is specified and the read-out access mode is specified, while each address with which Memory 4A-4D corresponds will be specified based on the assignment read-out address and the assignment read-out access mode and data will be read, the read data is outputted to coincidence.
[0033] For example, it is as follows when the 2 steps of line writing direction access mode as Address Cn (0) specified on the virtual minimum two-dimensional room 1 and shown in M3 in drawing 4 is specified now. That is, in this case, as for Address an (1) and memory 4B, as for Address cn (0) and memory 4D, Address dn (0) is specified, respectively, and Address bn (1) and memory 4C read [memory 4A] each of that data to coincidence.
[0034] Next, write-in actuation of the memory 4A-4D at the time of writing data in the address of the arbitration on the virtual minimum two-dimensional room 1 at coincidence is explained. In this case, while specifying the write-in address of that arbitration, the write-in access mode which specifies the write-in direction of data is specified. Then, while each address with which Memory 4A-4D corresponds is specified based on the assignment write-in address and the assignment write-in access mode and the writing of data is attained, the data which should be written in is written in coincidence to each of that address.
[0035] For example, it is as follows when the 2 steps of line writing direction access mode as Address Cn (0) specified on the virtual minimum two-dimensional room 1 and shown in M3 in drawing 4 is specified now. That is, in this case, as for Address an (1) and memory 4B, Address dn (0) is specified, respectively, as for Address cn (0) and memory 4D, the writing of data of it is attained, and Address bn (1) and memory 4C write [memory 4A] each of that data in coincidence.
[0036] If the access location and the access mode of arbitration on the two-dimensional room 3 are specified according to the operation of the memory concerning this operation gestalt as explained above, according to that assignment, the data which follow the longitudinal direction or lengthwise direction of arbitration on the two-dimensional room 3 from an access location can be written in each memory 4A-4D at coincidence. For this reason, the operation of the memory concerning this operation gestalt can be contributed to the increase in efficiency of a SIMD operation.
[0037] Next, the configuration of the operation gestalt of the two-dimensional data access memory of this invention is explained with reference to drawing 5 - drawing 7 . The two-dimensional data access memory 10 concerning this operation gestalt materialized the operation of the memory concerning the operation gestalt mentioned above, and as shown in drawing 5 , it is equipped with Memory 4A-4D, the read-out address control section 11, the read-out data control section 12, the write-in address control section 13, and the write-in data control section 14. And while it reads with the read-out address control section 11 and the data control section 12 constitutes a data read-out system, it writes in with the write-in address control section 13, the data control section 14 constitutes a data write-in system, and these two systems share Memory 4A-4D.
[0038] Supposing the two-dimensional room 3 which arranged the virtual minimum two-dimensional room 1 which shows Memory 4A-4D to drawing 1 in the direction in every direction as shown in drawing 3 , each address of the virtual minimum two-dimensional room 1 is beforehand assigned to the predetermined address under a fixed regulation, respectively, as shown in drawing 2 . While the read-out address control section 11 changes the predetermined address of the read-out address into a predetermined value and outputs it to Memory 4A-4D according to assignment of the read-out access mode in the case of

assignment of the read-out address In straddling the virtual minimum two-dimensional room 1 where the space to access adjoins, according to (drawing 3 , refer to drawing 4), and the assignment read-out access mode, the addresses other than the above of the read-out address are amended, and it outputs to Memory 4A-4D.
[0039] the read-out data control section 12 -- the time of read-out of data -- a part of read-out address -- being based -- the read-out address on the virtual minimum two-dimensional room 1 -- specifying -- this -- it was specified -- it reads and they are the address and the specified thing which reads, rearranges each read-out data from Memory 4A-4D according to the access mode, and outputs each of this rearranged read-out data to coincidence.
[0040] While the write-in address control section 13 changes the predetermined address of the write-in address into a predetermined value and outputs it to Memory 4A-4D according to assignment of the write-in access mode in the case of assignment of the write-in address In straddling the virtual minimum two-dimensional room 1 where the space to access adjoins, according to the assignment write-in access mode, the addresses other than the above of the write-in address are amended, and it outputs to Memory 4A-4D.
[0041] In case the write-in data control section 14 writes in each data to Memory 4A-4D Based on a part of write-in address, the write-in address on the virtual minimum two-dimensional room 1 is specified. They are this specified write-in address and the specified thing which is controlled to write in, to rearrange each write-in data to Memory 4A-4D, and to write each of this write-in rearranged data in each appointed address of Memory 4A-4D at coincidence according to the access mode.
[0042] Next, it reads with the read-out address control section 11 shown in drawing 5 , and the detailed configuration of the data control section 12 is explained with reference to drawing 6 . The read-out address control section 11 is equipped with the address controller 21 and the four address amendment sections 22A-22D as shown in drawing 6 . Read the address controller 21 with assignment of the read-out addresses A0 and A1, A4, and A5, and it responds to assignment of the access mode. While outputting the address translation signal for changing read-out address A4 and A5 equivalent to the addresses a0 and a1 of 2 bits of low order of Memory 4A-4D into a predetermined value to the address amendment sections 22A-22D In straddling the virtual minimum two-dimensional room 1 where the space to access adjoins The amendment signal for amending the read-out address A2 equivalent to the addresses a2-a7 of 5 bits of high orders of Memory 4A-4D, A3, and A6 - A9 to a predetermined value according to assignment of the read-out access mode is outputted to the address amendment sections 22A-22D.
[0043] Here, the above-mentioned read-out address "A0, A1" specifies the address of the line writing direction (longitudinal direction) of the virtual minimum two-dimensional room 1, and is equivalent to the addresses a0 and a1 by the side of the low order of Memory 4A-4D. Moreover, the read-out address "A4, A5" specifies the address of the direction of a train of the virtual minimum two-dimensional room 1 (lengthwise direction). Furthermore, the read-out address A2, A3, and A6 - A9 specify the address of the two-dimensional room 3, and are equivalent to the addresses a2-a7 of Memory 4A-4D.
[0044] The address amendment sections 22A-22D are formed corresponding to Memory 4A-4D. While reading with the address translation signal from the address controller 21, changing address A4 and A5 into a predetermined value and outputting as the addresses a0 and a1 of the lower bit of each memory 4A-4D It reads with the amendment signal from the address controller 21, only a predetermined value amends the address A2, A3, and A6 - A9, and it outputs as the addresses a2-a7 of 5 bits of high orders of Memory 4A-4D.
[0045] The read-out data control section 12 is equipped with the data controller 23 and four selectors 24A-24D as shown in drawing 6 . The data controller 23 specifies the read-out address on the virtual minimum two-dimensional room 1 according to assignment of the read-out addresses A0 and A1, A4, and A5 in the case of read-out of data. According to the read-out access mode which specifies this specified direction that reads and reads data from the address, the selection signal at the time of Selectors 24A-24D choosing Memory 4A-4D is outputted to Selectors 24A-24D, respectively.
[0046] Selectors 24A-24D are formed corresponding to Memory 4A-4D, choose the read-out data on output Rhine of each memory 4A-4D based on the above-mentioned selection signal of the data controller 23, and output them to coincidence (it takes out). Next, it writes in with the write-in address control section 13 shown in drawing 5 , and the detailed configuration of the data control section 14 is explained with reference to drawing 7 .
[0047] The write-in address control section 13 is equipped with the address controller 31 and the four address amendment sections 32A-32D as shown in drawing 7 . Write in the address controller 31 with assignment of the write-in addresses A0 and A1, A4, and A5, and it responds to assignment of the access mode. While outputting the address translation signal for changing write-in address A4 and A5 equivalent

to the addresses a0 and a1 of 2 bits of low order of Memory 4A-4D into a predetermined value to the address amendment sections 32A-32D In straddling the virtual minimum two-dimensional room 1 where the space to access adjoins An amendment signal only for a predetermined value to amend the write-in address A2 equivalent to the addresses a2-a7 of 5 bits of high orders of Memory 4A-4D, A3, and A6 - A9 according to assignment of the write-in access mode is outputted to the address amendment sections 32A-32D.

[0048] Here, the write-in access mode is fundamentally [as the above-mentioned read-out access mode] the same, and consists of the three access modes. The address amendment sections 32A-32D are formed corresponding to Memory 4A-4D. While writing in with the address translation signal from the address controller 31, changing address A4 and A5 and outputting as the addresses a0 and a1 of 2 bits of low order of each memory 4A-4D It writes in with the amendment signal from the address controller 31, the address A2, A3, and A6 - A9 are amended, and it outputs as the addresses a2-a7 of 5 bits of high orders of Memory 4A-4D.

[0049] The write-in data control section 14 is equipped with the data controller 33 and four selectors 34A-34D as shown in drawing 7 . The data controller 33 specifies the write-in address on the virtual minimum two-dimensional room 1 according to assignment of the write-in addresses A0 and A1, A4, and A5 in the case of the writing of data, and it writes in and it outputs the selection signal at the time of Selectors 34A-34D choosing Memory 4A-4D from the address according to the write-in access mode which specifies this specified direction that writes in data to Selectors 34A-34D, respectively.

[0050] Selectors 34A-34D are formed corresponding to Memory 4A-4D, and supply the write-in data (for example, 32 bits) from the outside to coincidence by 8 bitwises as opposed to each appointed address of each memory 4A-4D based on the above-mentioned selection signal of the data controller 33. Next, actuation of the two-dimensional data access memory concerning the operation gestalt which consists of such a configuration is explained with reference to drawing 8 - drawing 10 .

[0051] First, the case where data are read is explained. In this case, the data controller 23 and the read data based on Selectors 24A-24D need control of the read-out address by the address controller 21 and the address amendment sections 22A-22D, and to be controlled, and sequence of explanation is performed from the data controller 23. The data controller 23 shown in drawing 6 outputs the selection signal at the time of Selectors 24A-24D choosing Memory 4A-4D to Selectors 24A-24D according to the read-out access mode, respectively while specifying the read-out address on the virtual minimum two-dimensional room 1 according to assignment of the read-out addresses A0 and A1, A4, and A5 in the case of read-out of data.

[0052] For example, as shown in No1 of drawing 8 , when "00" and "00" are specified as the read-out address "A0, A1", and "A4, A5" and the line writing direction access mode (00) is specified as the read-out access mode, as for memory 4A and selector 24B, memory 4C and selector 24D choose memory 4D for selector 24A, respectively, as for memory 4B and selector 24C.

[0053] As shown in No17 of drawing 8 , for example, moreover, the read-out address "A0, A1", When "00" and "00" are specified as "A4, A5" and the direction access mode of a train (01) is specified as the read-out access mode selector 24A -- memory 4A -- selector 24C chooses memory 4B, and, as for selector 24D, selector 24B chooses memory 4D for memory 4C, respectively.

[0054] Selectors 24A-24D output the read-out data on output Rhine of each memory 4A-4D to coincidence based on the selection signal from the data controller 23 in the case of read-out of data. For example, as for each output Rhine up read-out data (for example, 8 bits) of Memory 4A-4D, in the case of No1 of drawing 8 , memory 4D data are outputted by selector 24A as mentioned above at coincidence by the data of memory 4A, the data which are memory 4C by the data of memory 4B, and selector 24C in selector 24B, and selector 24D in the case of read-out of data. Moreover, as for each output Rhine up read-out data of Memory 4A-4D, in the case of No17 of drawing 8 , memory 4D data are outputted by selector 24A at coincidence by the data of memory 4A, the data which are memory 4B by the data of memory 4C, and selector 24C in selector 24B, and selector 24D in the case of read-out of data.

[0055] On the other hand, the address controller 21 outputs the address translation signal for changing into a predetermined value the read-out addresses A0 and A1, A4, read-out address A4 that reads with assignment of A5 and is equivalent to the addresses a0 and a1 of 2 bits of low order of Memory 4A-4D according to assignment of the access mode, and A5 to the address amendment sections 22A-22D, respectively.

[0056] For example, as shown in drawing 9 , when the line writing direction access mode is specified as the read-out access mode and the read-out address "A4, A5" is specified, conversion of the assignment read-out address "A4, A5" is not performed. When therefore, read-out address "A4 and A5" are specified

as "00", the "00" is outputted as each address of 4A-4D of memory "a0, a1."
[0057] On the other hand, as shown in drawing 9 , when the direction access mode of a train or the 2 steps of line writing direction access mode is specified for the read-out access mode and the read-out address "A4, A5" is specified, conversion of the assignment read-out address "A4, A5" is performed. for example, when the direction access mode of a train is specified as the read-out access mode and the read-out address "A4, A5" is specified as "00" Although not changed about the address "a0, a1" of memory 4A, about each address "a0, a1" of Memory 4B, 4C, and 4D, it is changed into "01", "10", and "11", respectively, and is outputted to them.
[0058] When straddling the virtual minimum two-dimensional room 1 where the space to access adjoins, the address controller 21 (drawing 3 and drawing 4 Furthermore, reference), According to assignment of the read-out access mode, output the read-out address A2 to specify, A3, and A6 - A9 as it is as the address equivalent to the addresses d2-d7 of 5 bits of high orders of Memory 4A-4D, or Or that read-out address A2 to specify, A3, and A6 - A9 are amended, and the amendment signal which outputs this amended address as the addresses d2-d7 of 5 bits of high orders of Memory 4A-4D is outputted to the address amendment sections 22A-22D.
[0059] For example, as shown in No2 of drawing 10 , when the line writing direction access mode is specified as the read-out access mode and "1000" is specified as the read-out addresses A0 and A1, A4, and A5, the address controller 21 outputs the amendment signal for carrying out "+1" addition of the addresses a2-a7 of memory 22A to address amendment section 22A. Therefore, "+1" in drawing 10 and "+4" mean that "+1" and "+4" addition of the addresses a2-a7 of memory 22A are carried out.
[0060] Next, the case where data are written in is explained. In this case, the address controller 31, control of the write-in address by the address amendment sections 32A-32D, and the data controller 33 and control of the read-out data based on Selectors 34A-34D are required. However, since actuation of control of the write-in address by the address controller 31 and the address amendment sections 32A-32D is substantially [as the above-mentioned address controller 21 and actuation of control of the read-out address by the address amendment sections 22A-22D] the same, the explanation is omitted.
[0061] The data controller 33 specifies the write-in address on the virtual minimum two-dimensional room 1 according to assignment of the write-in addresses A0 and A1, A4, and A5 in the case of the writing of data, and it writes in and it outputs the selection signal at the time of Selectors 34A-34D choosing Memory 4A-4D from the address according to the write-in access mode which specifies this specified direction that writes in data to Selectors 34A-34D, respectively. In addition, this data controller 33 is fundamentally [as actuation of the data controller 23] the same.
[0062] Moreover, based on the selection signal from the data controller 33, Selectors 34A-34D choose each write-in data from the outside, and supply it to the appointed address of each memory 4A-4D at coincidence. As explained above, according to the two-dimensional data access memory concerning this operation gestalt Upwards, can read to coincidence the continuation data located in a line with the longitudinal direction or the lengthwise direction from the specified location on two-dimensional room from the physical memory 4A-4D, and Since it can write in each memory 4A-4D at coincidence so that data may be continuously located in a line with a longitudinal direction or a lengthwise direction from the specified location on two-dimensional room, an efficient SIMD operation becomes realizable.
[0063] Next, the configuration of the operation gestalt of the processing unit of this invention is explained with reference to drawing 11 . The processing unit concerning this operation gestalt applies the two-dimensional data access memory 10 shown in drawing 5 - drawing 7 , and it is made to make two-dimensional DCT (two-dimensional discrete KOSANIN conversion) perform to the SIMD mold processor 41.
[0064] For this reason, as this processing unit is shown in drawing 11 , the SIMD mold processor 41 and the external I/F circuit 42 are connected to the two-dimensional data access memory 10. The SIMD mold processor 41 is a processor which can be set up by the instruction program about the above-mentioned access mode while being able to specify reading of the data in the two-dimensional data access memory 10, or the address in the case of writing according to predetermined data processing like the after-mentioned. Moreover, the external I/F circuit 41 delivers and receives data with the exterior.
[0065] Next, the example of the processing unit concerning the operation gestalt which consists of such a configuration of operation is explained. First, the pixel data of 8 RA 8 which serve as an object which performs two-dimensional DCT by the external I/F circuit 42 are written in the two-dimensional data access memory 10, as shown in drawing 12 .
[0066] Next, the SIMD mold processor 41 performs 1-dimensional DCT to a line writing direction. For this reason, as shown in drawing 12 , pixel data of even lines and odd lines are read into a pair, and the

SIMD mold processor 41 reads two pixel data in the direction of a train, and changes 1-dimensional DCT for two lines into coincidence by the SIMD operation. And as shown in drawing 13 , the result of 1-dimensional DCT of a line writing direction is returned to the two-dimensional data access memory 10.
[0067] Furthermore, the SIMD mold processor 41 performs 1-dimensional DCT of the direction of a train. In this case, as shown in drawing 13 , an odd number train is read into a pair, two pixel data are read into a line writing direction for an even number train, 1-dimensional DCT for two trains is changed into coincidence by the SIMD operation, and that result is again returned to the two-dimensional data access memory 10. Thereby, the result of final two-dimensional DCT as shown in drawing 14 is obtained on the two-dimensional data access memory 10. Consequently, it outputs outside via the external I/F circuit 42 again.
[0068] Since the two-dimensional data access memory concerning this operation gestalt is used according to the processing unit concerning this operation gestalt as explained above, a SIMD operation can be performed efficiently.
(Gestalt of the 2nd operation) Next, the gestalt of operation of the 2nd of this invention is explained with reference to a drawing.
[0069] In the operation of the memory concerning the gestalt of this operation, the virtual two-dimensional room 1 as shown in drawing 1 is appointed like the gestalt of the 1st operation, and the two-dimensional room 3 as shown in drawing 3 is assumed. Hereafter, the operation of the memory concerning the gestalt of this operation is explained. First, the two-dimensional room 3 which arranged the virtual minimum two-dimensional room 1 as shown in drawing 1 in the shape of a tile in the direction in every direction as shown in drawing 3 is assumed.
[0070] On the other hand, each address of the virtual minimum two-dimensional room 1 is beforehand assigned to each four physical predetermined address of Memory 4A-4D decided by relation with the magnitude of the virtual minimum two-dimensional room 1, and is set to it (refer to drawing 1 and drawing 2). (matching) Next, the read-out actuation from the memory 4A-4D at the time of reading continuous or nonsequential predetermined data from the address of the arbitration on the virtual minimum two-dimensional room 1 is explained.
[0071] In this case, while specifying the read-out address of that arbitration, the read-out access mode which specifies the read-out direction of data is specified. In addition to the same line writing direction access mode as the gestalt of the 1st operation, the direction access mode of a train, and the 2 steps of line writing direction access mode, there is the alternate mode in this read-out access mode. Furthermore, in the memory operation concerning the gestalt of this operation, the option mode which shows the memory operation in motion vector presumption of a dynamic image is specified.
[0072] There is circular mode and padding mode among these option modes. Hereafter, each option mode and the alternate mode are explained. As shown in drawing 15 , the circular mode is the mode for performing motion vector presumption efficiently, when data are referred to in presumption of a motion vector ranging over the storage region of the two-dimensional room 3.
[0073] That is, the fixed field (refer to drawing 16) of the reference frame which adjoins the present frame and a time amount target is memorized in the two-dimensional room 3 in the case of motion vector presumption. And retrieval (block matching) of the block for attention of the present frame and the block (block approximated most) which is the minimum error is performed out of the data memorized in the two-dimensional room 3. At this time, the field of the two-dimensional room 3 which retrieval ended is overwritten in the circular mode to the timing which mentions later current and the line writing direction data which follow the data of the reference frame memorized in the two-dimensional room 3, i.e., the data contiguous to the right-hand side of the storage region of the two-dimensional room 3. That is, in the two-dimensional room 3, the data of the line writing direction which continues from the storage region of the two-dimensional room 3 in a reference frame are cyclically memorized to data [finishing / reference].
[0074] And in the two-dimensional room 3, a retrieval object domain (block) is moved serially. When the data over the boundary of the field memorized in the two-dimensional room 3 are referred to, about the data referred to across the boundary (right end) of the storage region of the two-dimensional room 3 By amending the address of the data to refer to, motion vector presumption is performed with reference to the data (predetermined data memorized cyclically) of the predetermined address overwritten by the two-dimensional room 3. Therefore, since, as for a user, he does not need to be conscious of whether a retrieval object domain straddles the boundary of the two-dimensional room 3 in the case of the circular mode, motion vector presumption can be performed efficiently.
[0075] Here, the approach of processing of performing motion vector presumption in the circular mode is explained. Drawing 17 is a flow chart which expresses the processing for performing motion vector

presumption in the circular mode. In drawing 17 , if the circular mode is specified and motion vector presumption is started, the range for retrieval in a reference frame will be set up, and the address which reads the data of the virtual minimum two-dimensional room 3 will be initialized (step S10).
[0076] Next, block matching is performed with reference to the data read from the predetermined address (step S20), and it judges whether block matching was ended about all the range for retrieval (step S30). In step S30, when it judges with having not ended block matching about all the range for retrieval, it judges whether block matching is completed about all the data in the virtual minimum two-dimensional room 1 (step S40).
[0077] In step S40, when it judges with block matching being completed about no data in the virtual minimum two-dimensional room 1, in order to perform block matching about unsettled data, the read-out address of the virtual minimum two-dimensional room 1 is updated (step S50), and it shifts to step S20. On the other hand, when it judges with block matching being completed about all the data in the virtual minimum two-dimensional room 1 in step S40, from what block matching has ended about the virtual minimum two-dimensional room 1 (it is reference ending), new reference data (for example, line writing direction data which adjoin in a reference frame) are overwritten (step S60), and it shifts to processing of step S50.
[0078] In step S30, when it judges with having ended block matching about all the range for retrieval, motion vector presumption processing is ended. Next, padding mode is explained. Padding mode is the mode for performing motion vector presumption appropriately, when the boundary of the storage region of the two-dimensional room 3 is in the condition which is in agreement with the image boundary (for example, the right end and lower limit of an image) of a reference frame in presumption of a motion vector, as shown in drawing 18 .
[0079] That is, in the two-dimensional room 3, a retrieval object domain (block) is serially moved in the case of motion vector presumption. At this time, the boundary of the storage region of the two-dimensional room 3 is in the condition which is in agreement with the boundary part of a reference frame (refer to drawing 18), and when the data over the boundary of this storage region are referred to, the data referred to across the boundary (a right end or lower limit) of a storage region are data which originally do not exist. So, in padding mode, motion vector presumption is performed with reference to the data (namely, data memorized in the right end and lower limit of the two-dimensional room 3) of the boundary memorized in the two-dimensional room 3 about the data referred to across the boundary (a right end or lower limit) of a storage region. That is, about the data referred to across the boundary (a right end or lower limit) of a storage region, bordering data are complemented on the periphery of the image boundary of a reference frame, and the data is referred to on it. therefore, the case where the boundary of the storage region of the two-dimensional room 3 is in the condition which is in agreement with the image boundary of a reference frame in the case of padding mode -- suitable -- motion vector presumption -- a line -- things are made.
[0080] In addition, in the gestalt of this operation, although the case where data were referred to across the boundary of the storage region of the right end of the two-dimensional room 3 or a lower limit was mentioned as the example and explained, this invention is applicable about the case where data are referred to across the boundary of the storage region of the upper limit of the two-dimensional room 3, or a left end, similarly. In this case, the same processing as **** is realizable by changing the correction value shown in drawing 25 into the value which suits when data are referred to across the boundary of the storage region of the upper limit of a storage region, or a left end.
[0081] Next, the alternate mode is explained. The alternate mode is the mode inputted as one of the read-out access modes, and as shown in drawing 19 , it is the mode for performing block matching at a high speed in presumption of a motion vector. That is, the fixed field of the reference frame which adjoins the present frame and a time amount target is memorized in the two-dimensional room 3 in the case of motion vector presumption. And a total of 4 pixels of the data of the 1st train of the 1st line and each 3rd line and the 3rd train of the 4x4-pixel data of the virtual minimum two-dimensional room 1 in the two-dimensional room 3 are read, and block matching is performed to these data. Such processing is performed about each virtual minimum two-dimensional room 1 of the two-dimensional room 3. Such processing is repeated changing the address of the pixel data to read in the virtual minimum two-dimensional room 1, similarly, as shown in drawing 20 . Then, block matching for all pixels can be performed and the block which is the minimum error correctly can be searched.
[0082] Here, in case block matching is performed, it judges that the block with which the accumulation remainder of each pixel data of the block for attention and each pixel data referred to serves as min is a block approximated most. Moreover, in case block matching in the alternate mode is performed, as shown

in drawing 20 , block matching for all pixel data can be performed by performing four block matching. As shown in drawing 21 in the alternate mode at this time, the threshold over the accumulation remainder according to the count of activation of block matching is set up, and when the accumulation remainder of each pixel data contained in each block exceeds a threshold, block matching of that block is stopped and it shifts to block matching of the following pixel data. Therefore, since it is not necessary to perform block matching of all pixels, block matching to the data memorized in the two-dimensional room 3 can be performed at a high speed. That is, a motion vector can be presumed at a high speed. In addition, although the pattern of reading of pixel data which performs block matching is shown in drawing 19 and drawing 20 , it can be performed with the pattern started from the address of others and arbitration.

[0083] That in addition, thresholds d1, d2, and d3 are in a predetermined price increase time in drawing 21 from the straight line which connected 0 (zero) andd4 When it is the block matching process in the alternate mode, for example, (a) of drawing 20 was read Since the remainder is over the value of an above-mentioned straight line, it is for avoiding the situation of omitting the block which serves as the minimum error by subsequent processing (it removing from the object of block matching if it is not the minimum error).

[0084] Thus, if the read-out address of the arbitration on the virtual minimum two-dimensional room 1 is specified and the read-out access mode and option mode are specified, while each address with which Memory 4A-4D corresponds will be specified based on the assignment read-out address, the assignment read-out access mode, and assignment option mode and data will be read, the read data is outputted to coincidence.

[0085] For example, it is as follows when the line writing direction access mode and the circular mode as the address a03 (2) specified on the virtual minimum two-dimensional room 1 and shown in M3 in drawing 15 are specified now. That is, in this case, as for the address a03 (2) and memory 4B, as for the address c03 (2) and memory 4D, the address d03 (2) is specified, respectively, and the address b04 (2) and memory 4C read [memory 4A] each of that data to coincidence. At this time, it is the same line address of the two-dimensional room 3, the left end address is matched with the address b04 of memory 4B (2) like the after-mentioned, and the data of the address b04 of memory 4B (2) are read by being accessed to the address at the left end of the same line address of the two-dimensional room 3.

[0086] Moreover, it is as follows when the line writing direction access mode and padding mode as the address d03 (2) specified on the virtual minimum two-dimensional room 1 and shown in M3, for example in drawing 18 are specified. That is, in this case, data are not read from memory 4A and memory 4B, but in memory 4C, the address d03 (2) is specified, respectively and the address c03 (2) and memory 4D read each of that data to coincidence. At this time, bordering data, i.e., the data of the address c03 of memory 4C (2), are read about the part beyond an image boundary.

[0087] Moreover, it is as follows, when Address an (0) is specified on the virtual minimum two-dimensional room 1 and the alternate mode is specified in drawing 19 for example. That is, in this case, as for Address an (0) and memory 4B, as for Address cn (0) and memory 4D, Address dn (2) is specified, respectively, and Address bn (2) and memory 4C read [for example, memory 4A] each of that data to coincidence. In addition, as shown in drawing 20 , in case block matching is performed further, the predetermined address is specified and each data is read.

[0088] If according to the operation of the memory in the gestalt of this operation it reads with the access location of the arbitration on the two-dimensional room 3 and the access mode and option mode are specified as explained above, according to that assignment, each processing (processing specified in circular mode and padding mode and the alternate mode) in presumption of a motion vector will be performed. For this reason, the operation of the memory concerning the gestalt of this operation can be contributed to the increase in efficiency of the SIMD operation about presumption of a motion vector.

[0089] Next, the configuration of the operation gestalt of the two-dimensional data access memory of this invention is explained with reference to drawing 22 and drawing 23 . That fundamental configuration of the two-dimensional data access memory 100 concerning this operation gestalt is the same as that of the two-dimensional data access memory [in / except for the point that the signal which materializes the operation of the memory concerning the operation gestalt mentioned above, and shows option mode to the read-out address control section 111 and the read-out data control section 112 is inputted / the gestalt of the 1st operation] 10 (refer to drawing 22). Therefore, only the different read-out address control section 111 and the different read-out data control section 112 which are a part are explained, the same number as the corresponding point of the two-dimensional data access memory 10 is attached about other parts, and explanation is omitted.

[0090] While the read-out address control section 111 changes the predetermined address of the read-out

address into a predetermined value and outputs it to Memory 4A-4D according to assignment of the read-out access mode in the case of assignment of the read-out address In straddling the virtual minimum two-dimensional room 1 where the space to access adjoins, according to (drawing 3 , refer to drawing 4), and the assignment read-out access mode, the addresses other than the above of the read-out address are amended, and it outputs to Memory 4A-4D.
[0091] Moreover, if data are referred to across the boundary (right end) of the storage region of the two-dimensional room 3 when the circular mode is inputted as option mode, about the data, the read-out address control section 111 will amend the address to refer to to the address of the predetermined data memorized cyclically, and will output it to Memory 4A-4D.
[0092] Moreover, the read-out address control section 111 will be instead outputted to Memory 4A-4D with reference to the address of the data of the boundary of a storage region about that data, if the data over the boundary of this storage region are referred to when padding mode is inputted as option mode and the boundary of the storage region of the two-dimensional room 3 is in the condition which is in agreement with the boundary part of a reference frame.
[0093] Furthermore, when the alternate mode is inputted as the read-out access mode, the read-out address control section 111 amends the address referred to in the virtual minimum room 1 to the address of a predetermined reference pattern (refer to drawing 19), and outputs it to Memory 4A-4D. the read-out data control section 112 -- the time of read-out of data -- a part of read-out address -- being based -- the read-out address on the virtual minimum two-dimensional room 1 -- specifying -- this -- it was specified -- it reads and they are the address and the specified thing which reads, rearranges each read-out data from Memory 4A-4D according to the access mode and option mode, and outputs each of this rearranged read-out data to coincidence.
[0094] Next, it reads with the read-out address control section 111 shown in drawing 22 , and the detailed configuration of the data control section 112 is explained with reference to drawing 23 . The read-out address control section 111 is equipped with the address controller 121 and the four address amendment sections 22A-22D as shown in drawing 23 . Read the address controller 121 with a part of read-out address A0 - A9, or all assignment, and it responds to assignment in the access mode and option mode. While outputting the address translation signal for changing read-out address A4 and A5 equivalent to the addresses a0 and a1 of 2 bits of low order of Memory 4A-4D into a predetermined value to the address amendment sections 22A-22D When straddling the virtual minimum two-dimensional room 1 where the space to access adjoins, and when the circular mode is specified as option mode The amendment signal for amending the read-out address A2 equivalent to the addresses a2-a7 of 5 bits of high orders of Memory 4A-4D, A3, and A6 - A9 to a predetermined value according to assignment of the read-out access mode is outputted to the address amendment sections 22A-22D.
[0095] In addition, since the configuration of the address amendment sections 22A-22D is the same as that of the address amendment sections 22A-22D shown in drawing 6 , explanation is omitted. The read-out data control section 112 is equipped with the data controller 123 and four selectors 24A-24D as shown in drawing 23 . The data controller 23 specifies the read-out address on the virtual minimum two-dimensional room 1 according to a part of read-out address A0 - A9, or all assignment in the case of read-out of data. It responds to the option mode specified as the read-out access mode which specifies this specified direction that reads and reads data from the address. The selection signal at the time of Selectors 24A-24D choosing Memory 4A-4D is outputted to Selectors 24A-24D, respectively.
[0096] In addition, since the configuration of Selectors 24A-24D is the same as that of the selectors 24A-24D shown in drawing 6 , explanation is omitted. Next, actuation of the two-dimensional data access memory concerning the operation gestalt which consists of such a configuration is explained with reference to drawing 24 - drawing 28 . At this time, the data controller 123 and the read data based on Selectors 24A-24D need control of the read-out address by the address controller 121 and the address amendment sections 22A-22D, and to be controlled, when each option mode is inputted, and when the alternate mode is inputted as the read-out access mode, it divides, and address control and the read control of data are explained.
[0097] When the circular mode is inputted as option mode, the data controller 123 shown in drawing 23 While specifying the read-out address on the virtual minimum two-dimensional room 1 according to assignment of the read-out addresses A0 and A1, A4, and A5 According to the read-out access mode, the selection signal at the time of Selectors 24A-24D choosing Memory 4A-4D is outputted to Selectors 24A-24D, respectively.
[0098] Moreover, the address controller 121 shown in drawing 23 outputs the address translation signal for changing into a predetermined value the read-out addresses A0 and A1, A4, read-out address A4 that

reads with assignment of A5 and is equivalent to the addresses a0 and a1 of 2 bits of low order of Memory 4A-4D according to assignment of the access mode, and A5 to the address amendment sections 22A-22D, respectively.
[0099] Here, if the data over the boundary of the storage region of the two-dimensional room 3 are referred to, the address controller 121 will output the amendment signal for amending the address of the data to the address (address of the data memorized cyclically at the two-dimensional memory section 3) of predetermined data (conversion) to the address amendment sections 22A-22D. As shown in No2 of drawing 24 , for example, the read-out address "A0, A1", When "10" and "00" are specified as "A4, A5" and the line writing direction access mode (00) is specified as the read-out access mode In address amendment section 22A, "0" and address amendment section 22C output "0", and, as for address amendment section 22D, "-3" and address amendment section 22B output "0" as correction value, respectively.
[0100] In addition, when the direction access mode of a train or the 2 steps of directions access mode of a train is specified similarly and the two-dimensional room 3 consists of n bytes of length as shown in drawing 15 , to the address of the data referred to ranging over the boundary, "- (n-4)" is outputted in the direction of a train as correction value. Drawing 25 is drawing showing the address correction value after a high order triplet eye when the direction access mode of a train and the 2 steps of directions access mode of a train are specified.
[0101] Here, when the read-out address A0 - A9 are expressed by the sign-less two's complement, it will read, if the boundary (lower limit) of the two-dimensional room 3 is straddled in the direction of a train, and the address will return to "0." Therefore, it is not necessary to prepare the table of the contents shown in drawing 25 in this case. However, since it does not return to "0" also when the read-out address straddles the boundary (right end) of the two-dimensional room 3 in the case of the line writing direction access mode, it is necessary to prepare the table of the contents shown in drawing 24 .
[0102] When padding mode is inputted as option mode, next, the data controller 123 shown in drawing 23 While specifying the read-out address on the virtual minimum two-dimensional room 1 according to assignment of the read-out addresses A0 and A1, A4, and A5 According to the read-out access mode, the selection signal at the time of Selectors 24A-24D choosing Memory 4A-4D is outputted to Selectors 24A-24D, respectively.
[0103] As shown in No2 of drawing 26 , for example, the read-out address "A0, A1", When "10" and "00" are specified as "A4, A5" and the line writing direction access mode (00) is specified as the read-out access mode In memory 4C and selector 24C, memory 4D and selector 24D choose [selector 24A / memory 4B and selector 24B] memory 4D, respectively.
[0104] Moreover, the address controller 121 shown in drawing 23 outputs the address translation signal for changing into a predetermined value the read-out addresses A0 and A1, A4, read-out address A4 that reads with assignment of A5 and is equivalent to the addresses a0 and a1 of 2 bits of low order of Memory 4A-4D according to assignment of the access mode, and A5 to the address amendment sections 22A-22D, respectively.
[0105] Next, when the alternate mode is inputted as the read-out access mode, the data controller 123 shown in drawing 23 outputs the selection signal at the time of Selectors 24A-24D choosing Memory 4A-4D to Selectors 24A-24D, respectively while specifying the read-out address on the virtual minimum two-dimensional room 1 according to assignment of the read-out addresses A0 and A1, A4, and A5.
[0106] For example, as shown in No42 of drawing 27 , when "10" and "00" are specified as the read-out address "A0, A1", and "A4, A5", as for memory 4B and selector 24B, memory 4A and selector 24D choose memory 4C for selector 24A, respectively, as for memory 4D and selector 24C. Moreover, the address controller 121 shown in drawing 23 outputs the address translation signal for changing read-out address A4 and A5 equivalent to the addresses a0 and a1 of 2 bits of low order of Memory 4A-4D into a predetermined value according to assignment of the read-out addresses A0 and A1, A4, and A5 to the address amendment sections 22A-22D, respectively.
[0107] for example, as shown in No18 of drawing 28 , when "10" and "00" are specified as the read-out address "A0, A1", and "A4, A5" As for "01" and memory 4D, address amendment section 22A outputs correction value for "00" and memory 4C to set [memory 4A] the address of the addresses a0 and a1 of 2 bits of low order of Memory 4A-4D to "00" in "01" and memory 4B.
[0108] As explained above, according to the two-dimensional data access memory concerning this operation gestalt The data located in a line with discontinuity from the specified location on two-dimensional room in the alternate mode are read from the physical memory 4A-4D to coincidence. Also when block matching in motion vector presumption can be performed upwards and the data over the

boundary of the storage region of two-dimensional room are referred to in the circular mode, the data of the right address in a reference frame are referred to. Furthermore, in padding mode, also when data are referred to across the boundary of a reference frame, bordering data are complemented and the data is referred to. Therefore, efficient and suitable motion vector presumption is attained, and the efficient SIMD operation in the processing becomes realizable.

[0109] Next, the configuration of the operation gestalt of the processing unit of this invention is explained. the processing unit concerning this operation gestalt applies the two-dimensional data access memory 100 shown in drawing 22 and drawing 23 , and comes out having made motion vector presumption processing having made and perform to the SIMD mold processor 41. For this reason, as this processing unit is shown in drawing 29 , the SIMD mold processor 141 and the external I/F circuit 142 are connected to the two-dimensional data access memory 100.

[0110] The SIMD mold processor 141 is a processor which can be set up by the instruction program about the above-mentioned access mode and option mode while being able to specify reading of the data in the two-dimensional data access memory 100, or the address in the case of writing according to predetermined data processing like the after-mentioned. Moreover, the external I/F circuit 141 delivers and receives data with the exterior.

[0111] Next, the example of the processing unit concerning the operation gestalt which consists of such a configuration of operation is explained. Drawing 30 is a flow chart which shows actuation of motion vector presumption processing of the processing unit concerning the gestalt of this operation. In drawing 30 , a processing unit specifies the block which performs motion vector presumption in the present frame (step S101), and determines the range for retrieval based on a reference frame on the basis of the core of the block (step S102). In addition, drawing 31 is drawing showing the relation of the range for retrieval with the present frame and a reference frame, combines and shows the field memorized by the two-dimensional data access memory 100 in the range for retrieval.

[0112] And a processing unit reads a part of range for retrieval (henceforth a "local field") into the two-dimensional data access memory 100 (step S103), and judges that it is that the local field is completely included in the reference frame (the boundary is not crossed) (step S104). When it judges with the local field not being completely included in a reference frame in step S104, a processing unit It judges whether the range (protruded range) where the local field has exceeded the boundary of a reference frame is less than 3 pixels (step S105). When it judges with the range (protruded range) where the local field has exceeded the boundary of a reference frame being less than 3 pixels, Option mode is set as padding mode, and block matching is performed, referring to bordering data about the protruded range (step S106). And processing of a processing unit shifts to step S109.

[0113] When it judges with the range (protruded range) where the local field has exceeded the boundary of a reference frame not being less than 3 pixels in step S105, a processing unit From it being what refers to the range (4 pixels or more) which cannot be complemented in padding mode Option mode is set as a default mode (the circular mode and padding mode are not performed mode of usually processing), bordering data are complemented with another processing in the protruded range, and block matching is performed in it (step S108). And processing of a processing unit shifts to step S109.

[0114] When it judges with the local field being completely included in the reference frame in step S104, moreover, a processing unit Set option mode as the circular mode and to the storage region [finishing / reference] in the two-dimensional data access memory 100 The data which adjoin a local field in a reference frame are overwritten, and block matching is performed with reference to the overwritten predetermined data about the data referred to ranging over the boundary of a local field (step S108). And processing of a processing unit shifts to step S109.

[0115] finishing [a processing unit / after steps S106-S108 and a processing unit judge whether it retrieval(block-matching)-ends, comes out of all of the range for retrieval, and is (step S109), and / retrieval of all of the range for retrieval] -- it is not -- ** -- when it judges, a local field is updated in the range which searches continuously (step S110). And processing of a processing unit shifts to step S103.

[0116] In step S109, when it judges that all of the range for retrieval are retrieval ending, it judges whether as a result of block matching, the processing unit presumed the motion vector based on physical relationship with the block which was the minimum error of a reference frame (step S111), and motion vector presumption ended it about all blocks of the present frame (step S112).

[0117] In step S112, when it judges with motion vector presumption being completed about no blocks of the present frame, the location of the block which performs motion vector presumption of the present frame is updated (step S113), and it shifts to step S101. On the other hand, when it judges with motion vector presumption having been completed about all blocks of the present frame in step S112, motion

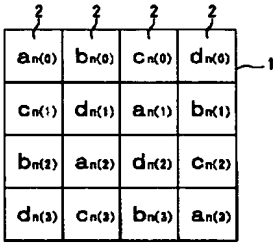
vector presumption processing is ended.
[0118] Since the two-dimensional data access memory concerning this operation gestalt is used according to the processing unit concerning this operation gestalt as explained above, efficient and suitable motion vector presumption is attained, and the efficient SIMD operation in that processing becomes realizable. As mentioned above, according to the two-dimensional data access memory concerning the 2nd operation gestalt of this invention The data located in a line with discontinuity from the specified location on two-dimensional room in the alternate mode are read from the physical memory 4A-4D to coincidence. Also when block matching in motion vector presumption can be performed upwards and the data over the boundary of the storage region of two-dimensional room are referred to in the circular mode, the data of the right address in a reference frame are referred to. Furthermore, in padding mode, also when data are referred to across the boundary of a reference frame, bordering data are complemented and the data is referred to. Therefore, efficient and suitable motion vector presumption is attained, and the efficient SIMD operation in the processing becomes realizable.
[0119] Furthermore, since the two-dimensional data access memory concerning the 2nd operation gestalt of this invention is used according to the processing unit concerning the 2nd operation gestalt of this invention, efficient and suitable motion vector presumption is attained, and the efficient SIMD operation in the processing becomes realizable. In addition, in the 1st and 2nd operation gestalten, although explained as inputting the signal line for specifying the access mode or option mode as a signal other than an address signal (a read-out address signal or write-in address signal), it is good also as packing the signal line for specifying the access mode or option mode with an address signal, and inputting it. For example, as shown in drawing 32 , it is good also as assigning the access mode or option mode to the most significant bit part of an address signal. Drawing 33 is the block diagram in which reading with the read-out address control section at the time of assigning a signal like drawing 32 , and showing the example of a configuration of the data control section.
[0120] the time of a user inputting the address, when it considers as such a configuration and processes using two-dimensional data access memory -- combining -- access mode **** -- being good -- since it is good only in inputting option mode, alter operation will become easier. Moreover, since the configuration of two-dimensional data access memory will become simpler, a circuit scale can be reduced and it becomes possible to raise a degree of integration etc.
[0121]
[Effect of the Invention] As explained above, according to the operation of the memory of this invention, it can contribute to the increase in efficiency of a SIMD operation. Moreover, since the continuation data or discontinuity data located in a line with the longitudinal direction or the lengthwise direction from the specified location on two-dimensional room can be read from each physical memory to coincidence according to the two-dimensional data access memory of this invention, an efficient SIMD operation becomes realizable.
[0122] Furthermore, since it can write in physical each memory at coincidence so that the continuation data which was located in a line with the longitudinal direction from the specified location on two-dimensional room or the lengthwise direction according to the two-dimensional data access memory of this invention can be read to coincidence upwards from physical each memory and data may be continuously located in a line with the longitudinal direction from the specified location on two-dimensional room, or a lengthwise direction, it becomes realizable [an efficient SIMD operation]. Moreover, it can contribute to the increase in efficiency of processing concerning motion vector presumption of a dynamic image.
[0123] Moreover, according to the processing unit of this invention, since the two-dimensional data access memory of this invention was used, a SIMD operation can be performed efficiently.

[Translation done.]

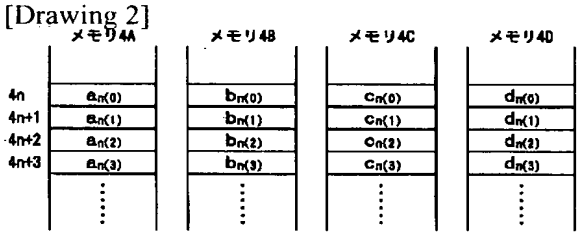
* NOTICES *

DRAWINGS

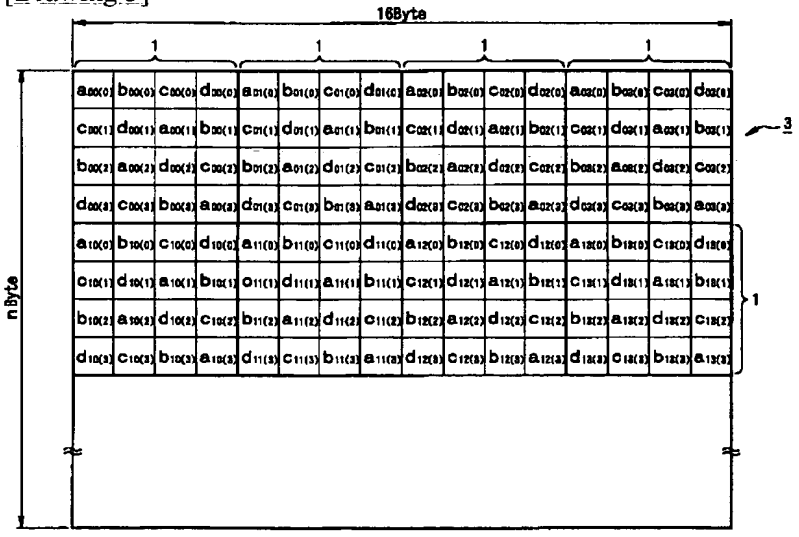
[Drawing 1]



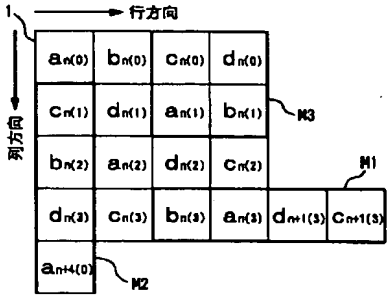
[Drawing 2]



[Drawing 3]



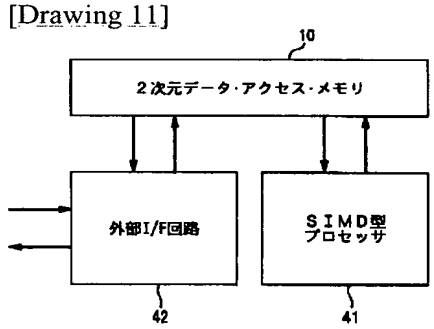
[Drawing 4]



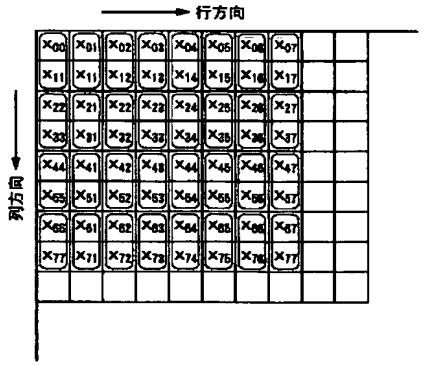
[Drawing 9]

読み出しアクセスモード	読み出しアドレス				メモリ4A		メモリ4B		メモリ4C		メモリ4D	
	A0	A1	A4	A5	a0	a1	a0	a1	a0	a1	a0	a1
行方向アクセスモード	−	−	0	0	0	0	0	0	0	0	0	0
	−	−	1	0	1	0	1	0	1	0	1	0
	−	−	0	1	0	1	0	1	0	1	0	1
	−	−	1	1	1	1	1	1	1	1	1	1
列方向アクセスモード	0	0	−	−	0	0	0	1	1	0	1	1
	1	0	−	−	0	1	0	0	1	1	1	0
	0	1	−	−	1	0	1	1	0	0	0	1
	1	1	−	−	1	1	1	0	0	1	1	1
列方向2段アクセスモード(16bit×2)	0	0	0	0	0	0	0	0	1	0	1	0
	0	0	1	0	0	1	0	1	1	0	1	0
	0	0	0	1	0	1	0	1	1	1	1	1
	0	0	1	1	0	0	0	0	1	1	1	1
	0	1	0	0	1	0	1	0	0	0	0	0
	0	1	1	0	1	0	1	0	0	1	0	1
	0	1	0	1	1	1	1	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	0	0	0

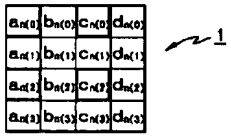
[Drawing 11]



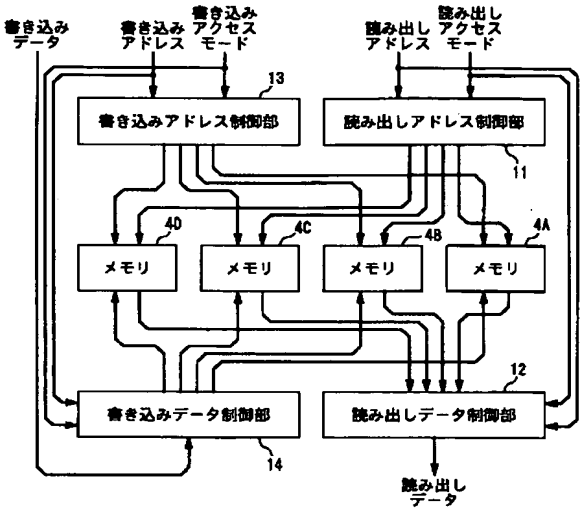
[Drawing 12]



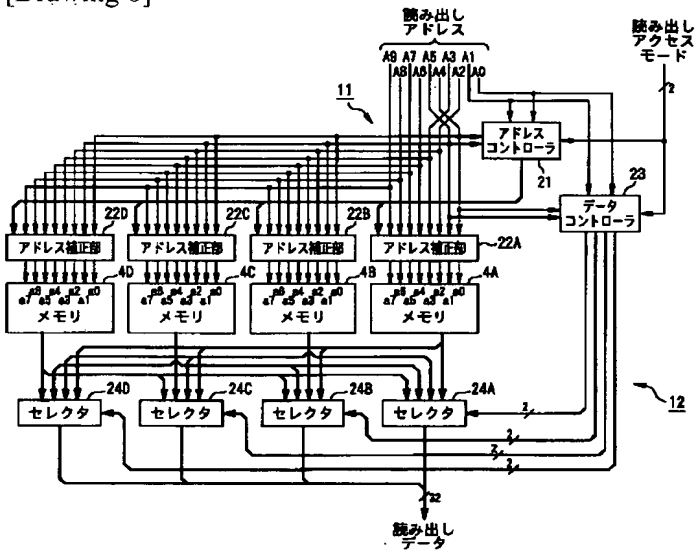
[Drawing 19]



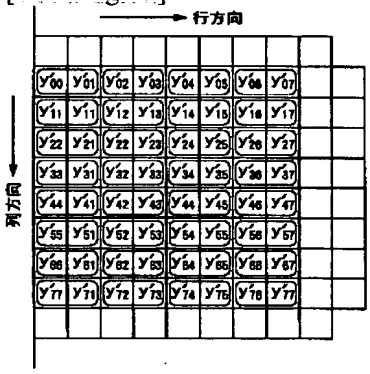
[Drawing 5]



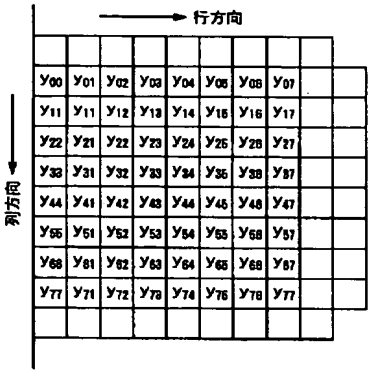
[Drawing 6]



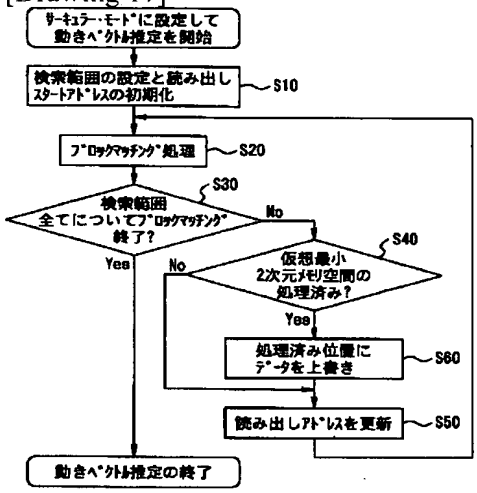
[Drawing 13]



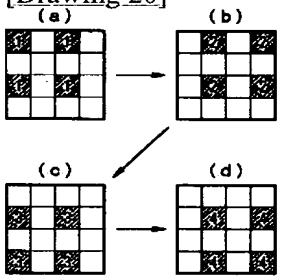
[Drawing 14]



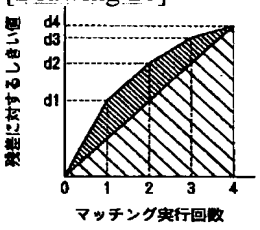
[Drawing 17]



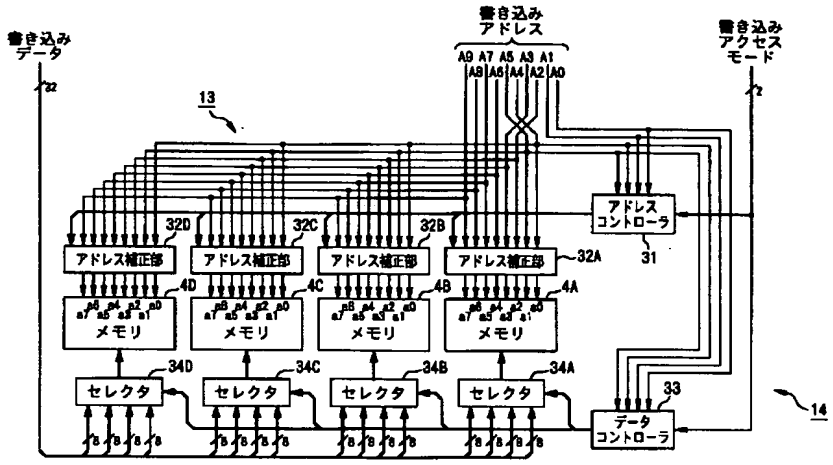
[Drawing 20]



[Drawing 21]



[Drawing 7]



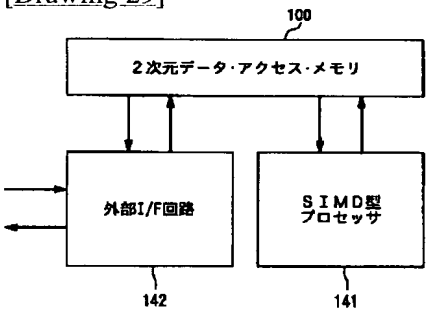
[Drawing 8]

No.	読み出し アクセスモード	読み出しアドレス A0	A1	A4	A5	セレクタ 24A	セレクタ 24B	セレクタ 24C	セレクタ 24D
1	行方向 アクセスモード (00)	0	0	0	0	4A	4B	4C	4D
2		1	0	0	0	4B	4C	4D	4A
3		0	1	0	0	4C	4D	4A	4B
4		1	1	0	0	4D	4A	4B	4C
5		0	0	1	0	4C	4D	4A	4B
6		1	0	1	0	4D	4A	4B	4C
7		0	1	1	0	4A	4B	4C	4D
8		1	1	1	0	4B	4C	4D	4A
9		0	0	0	1	4B	4A	4D	4C
10		1	0	0	1	4A	4D	4C	4B
11		0	1	0	1	4D	4C	4B	4A
12		1	1	0	1	4C	4B	4A	4D
13		0	0	1	1	4D	4C	4B	4A
14		1	0	1	1	4C	4B	4A	4D
15		0	1	1	1	4B	4A	4D	4C
16		1	1	1	1	4A	4D	4C	4B
17	列方向 アクセスモード (01)	0	0	0	0	4A	4C	4B	4D
18		1	0	0	0	4B	4D	4A	4C
19		0	1	0	0	4C	4A	4D	4B
20		1	1	0	0	4D	4B	4C	4A
21		0	0	1	0	4C	4B	4D	4A
22		1	0	1	0	4D	4A	4C	4D
23		0	1	1	0	4A	4D	4B	4C
24		1	1	1	0	4B	4C	4A	4D
25		0	0	0	1	4B	4D	4A	4C
26		1	0	0	1	4A	4C	4B	4D
27		0	1	0	1	4D	4B	4A	4C
28		1	1	0	1	4C	4A	4D	4B
29		0	0	1	1	4D	4A	4C	4B
30		1	0	1	1	4C	4B	4D	4A
31		0	1	1	1	4B	4C	4A	4D
32		1	1	1	1	4A	4D	4B	4C
33	列方向2段 アクセスモード 16bit×2 (10)	0	0	0	0	4A	4B	4C	4D
34		0	1	0	0	4C	4D	4A	4B
35		0	0	1	0	4C	4D	4B	4A
36		0	1	1	0	4A	4B	4D	4C
37		0	0	0	1	4B	4A	4D	4C
38		0	1	0	1	4D	4C	4B	4A
39		0	0	1	1	4D	4C	4A	4B
40		0	1	1	1	4B	4A	4C	4D

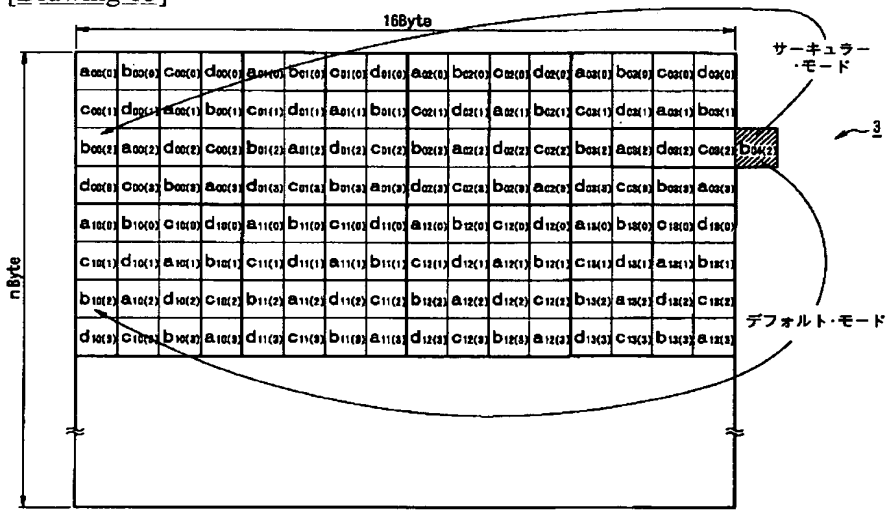
[Drawing 10]

No.	読み出しアクセスモード	読み出しアドレス A0	A1	A4	A5	アドレス補正部22A	アドレス補正部22B	アドレス補正部22C	アドレス補正部22D
1	行方向アクセスモード (00)	0	0	0	0	0	0	0	0
2		1	0	0	0	+1	0	0	0
3		0	1	0	0	+1	+1	0	0
4		1	1	0	0	+1	+1	+1	0
5		0	0	1	0	0	0	0	0
6		1	0	1	0	0	0	+1	0
7		0	1	1	0	0	0	+1	+1
8		1	1	1	0	+1	0	+1	+1
9		0	0	0	1	0	0	0	0
10		1	0	0	1	0	+1	0	0
11		0	1	0	1	+1	+1	0	0
12		1	1	0	1	+1	+1	0	+1
13		0	0	1	1	0	0	0	0
14		1	0	1	1	0	0	0	+1
15		0	1	1	1	0	0	+1	+1
16		1	1	1	1	0	+1	+1	+1
17	列方向アクセスモード (01)	0	0	0	0	0	0	0	0
18		1	0	0	0	0	0	0	0
19		0	1	0	0	0	0	0	0
20		1	1	0	0	0	0	0	0
21		0	0	1	0	+4	0	0	0
22		1	0	1	0	0	+4	0	0
23		0	1	1	0	0	0	+4	0
24		1	1	1	0	0	0	0	+4
25		0	0	0	1	+4	0	+4	0
26		1	0	0	1	0	+4	0	+4
27		0	1	0	1	+4	0	+4	0
28		1	1	0	1	0	+4	0	+4
29		0	0	1	1	+4	+4	+4	0
30		1	0	1	1	+4	+4	0	+4
31		0	1	1	1	+4	0	+4	+4
32		1	1	1	1	0	+4	+4	+4
33	列方向2段アクセスモード 16bit×2 (10)	0	0	0	0	0	0	0	0
34		0	1	0	0	0	0	0	0
35		0	0	1	0	0	0	0	0
36		0	1	1	0	0	0	0	0
37		0	0	0	1	0	0	0	0
38		0	1	0	1	0	0	0	0
39		0	0	1	1	+4	+4	0	0
40		0	1	1	1	0	0	+4	+4

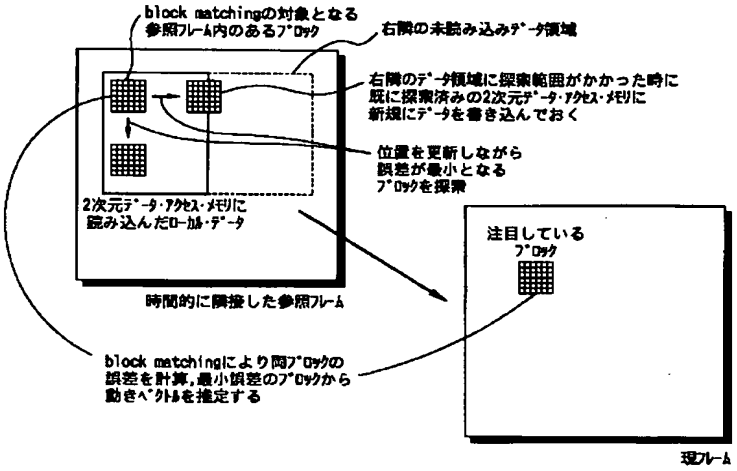
[Drawing 29]



[Drawing 15]



[Drawing 16]



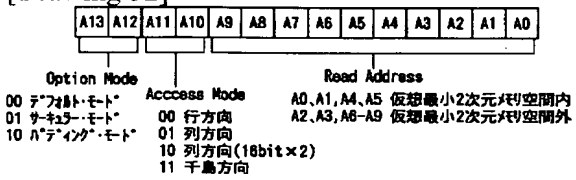
[Drawing 24]
(条件:サーキュラー・モード,かつA2=A3=1の時)

No.	読み出しアクセスモード	読み出しアドレス A0	A1	A4	A5	アドレス補正部22A	アドレス補正部22B	アドレス補正部22C	アドレス補正部22D
1	行方向アクセスモード(00)	0	0	0	0	0	0	0	0
2		1	0	0	0	-3	0	0	0
3		0	1	0	0	-3	-3	0	0
4		1	1	0	0	-3	-3	-3	0
5		0	0	1	0	0	0	0	0
6		1	0	1	0	0	0	-3	0
7		0	1	1	0	0	0	-3	-3
8		1	1	1	0	-3	0	-3	-3
9		0	0	0	1	0	0	0	0
10		1	0	0	1	0	-3	0	0
11		0	1	0	1	-3	-3	0	0
12		1	1	0	1	-3	-3	0	-3
13		0	0	1	1	0	0	0	0
14		1	0	1	1	0	0	0	-3
15		0	1	1	1	0	0	-3	-3
16		1	1	1	1	0	-3	-3	-3

[Drawing 28]

読み出しアクセスモード	読み出しアドレス A0	A1	A4	A5	メモリ4A a0	a1	メモリ4B a0	a1	メモリ4C a0	a1	メモリ4D a0	a1
行方向アクセスモード	−	−	0	0	0	0	0	0	0	0	0	0
	−	−	1	0	1	0	1	0	1	0	1	0
	−	−	0	1	0	1	0	1	0	1	0	1
	−	−	1	1	1	1	1	1	1	1	1	1
列方向アクセスモード	0	0	−	−	0	0	0	1	1	0	1	1
	1	0	−	−	0	1	0	0	1	1	1	0
	0	1	−	−	1	0	1	1	0	0	0	1
	1	1	−	−	1	1	1	0	0	1	1	1
列方向2段アクセスモード(16bit×2)	0	0	0	0	0	0	0	0	1	0	1	0
	0	0	1	0	0	1	0	1	1	0	1	0
	0	0	0	1	0	1	0	1	1	1	1	1
	0	0	1	1	0	0	0	0	1	1	1	1
	0	1	0	0	1	0	1	0	0	0	0	0
	0	1	1	0	1	0	1	0	0	1	0	1
	0	1	0	1	1	1	1	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	0	0	0
千鳥モード	0	0	0	0	0	0	0	1	0	0	0	1
	1	0	0	0	0	1	0	0	0	1	0	0
	0	1	1	0	1	0	1	1	1	0	1	1
	1	1	1	0	1	1	1	0	1	1	1	0

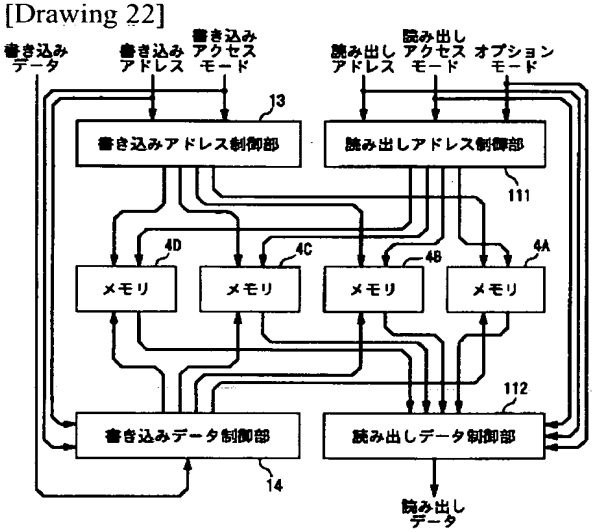
[Drawing 32]



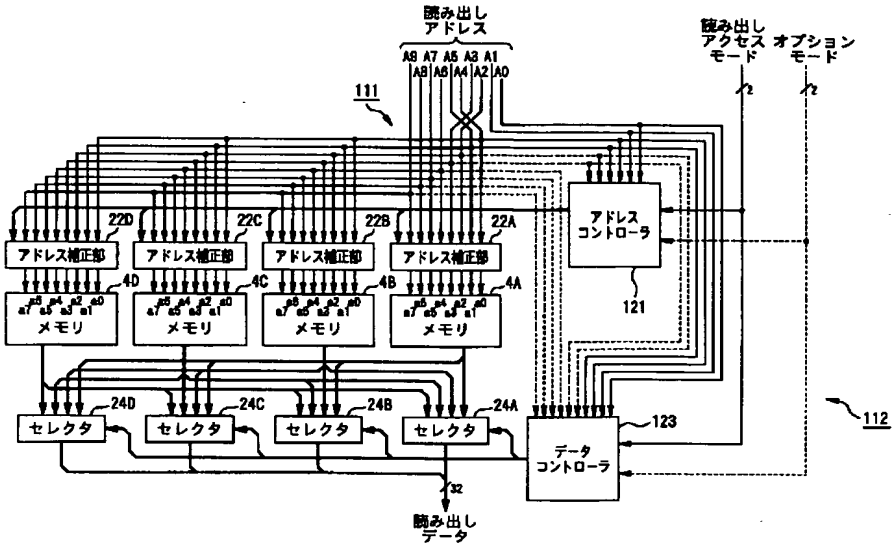
[Drawing 18]

ID=000020

[Drawing 22]



[Drawing 23]



[Drawing 25]
(条件:サーキュラー・モード,かつA6=A7=A8=A9=1の時)

No.	読み出しアクセスモード	読み出しアドレス A0	A1	A4	A5	アドレス補正部22A	アドレス補正部22B	アドレス補正部22C	アドレス補正部22D
17	列方向アクセスモード(01)	0	0	0	0	0	0	0	0
18		1	0	0	0	0	0	0	0
19		0	1	0	0	0	0	0	0
20		1	1	0	0	0	0	0	0
21		0	0	1	0	-(n-4)	0	0	0
22		1	0	1	0	0	-(n-4)	0	0
23		0	1	1	0	0	0	-(n-4)	0
24		1	1	1	0	0	0	0	-(n-4)
25		0	0	0	1	-(n-4)	0	-(n-4)	0
26		1	0	0	1	0	-(n-4)	0	-(n-4)
27		0	1	0	1	-(n-4)	0	-(n-4)	0
28		1	1	0	1	0	-(n-4)	0	-(n-4)
29		0	0	1	1	-(n-4)	-(n-4)	-(n-4)	0
30		1	0	1	1	-(n-4)	-(n-4)	0	-(n-4)
31		0	1	1	1	-(n-4)	0	-(n-4)	-(n-4)
32		1	1	1	1	0	-(n-4)	-(n-4)	-(n-4)
33	列方向2段アクセスモード18bit×2(10)	0	0	0	0	0	0	0	0
34		0	1	0	0	0	0	0	0
35		0	0	1	0	0	0	0	0
36		0	1	1	0	0	0	0	0
37		0	0	0	1	0	0	0	0
38		0	1	0	1	0	0	0	0
39		0	0	1	1	-(n-4)	-(n-4)	0	0
40		0	1	1	1	0	0	-(n-4)	-(n-4)

[Drawing 26]

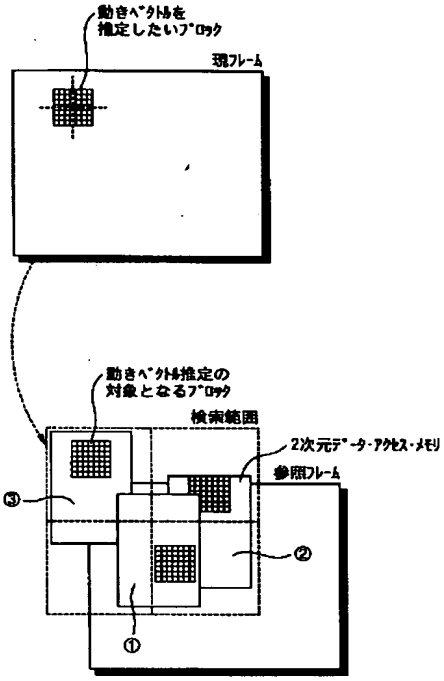
(条件:パディング・モードで,A2=A3=1,またはA6=A7=A8=A9=1の場合)

No.	読み出しアクセスモード	読み出しアドレス A0	A1	A4	A5	セレクタ 24A	セレクタ 24B	セレクタ 24C	セレクタ 24D
1	行方向アクセスモード (00)	0	0	0	0	4A	4B	4C	4D
2		1	0	0	0	4B	4C	4D	4D
3		0	1	0	0	4C	4D	4D	4D
4		1	1	0	0	4D	4D	4D	4D
5		0	0	1	0	4C	4D	4A	4B
6		1	0	1	0	4D	4A	4B	4B
7		0	1	1	0	4A	4B	4B	4B
8		1	1	1	0	4B	4B	4B	4B
9		0	0	0	1	4B	4A	4D	4C
10		1	0	0	1	4A	4D	4C	4C
11		0	1	0	1	4D	4C	4C	4C
12		1	1	0	1	4C	4C	4C	4C
13		0	0	1	1	4D	4C	4B	4A
14		1	0	1	1	4C	4B	4A	4A
15		0	1	1	1	4B	4A	4A	4A
16		1	1	1	1	4A	4A	4A	4A
17	列方向アクセスモード (01)	0	0	0	0	4A	4C	4B	4D
18		1	0	0	0	4B	4D	4A	4C
19		0	1	0	0	4C	4A	4D	4B
20		1	1	0	0	4D	4B	4C	4A
21		0	0	1	0	4C	4B	4D	4D
22		1	0	1	0	4D	4A	4C	4C
23		0	1	1	0	4A	4D	4B	4B
24		1	1	1	0	4B	4C	4A	4A
25		0	0	0	1	4B	4D	4D	4D
26		1	0	0	1	4A	4C	4C	4C
27		0	1	0	1	4D	4B	4B	4B
28		1	1	0	1	4C	4A	4A	4A
29		0	0	1	1	4D	4D	4D	4D
30		1	0	1	1	4C	4C	4C	4C
31		0	1	1	1	4B	4B	4B	4B
32		1	1	1	1	4A	4A	4A	4A
33	列方向2段アクセスモード 16bit×2 (10)	0	0	0	0	4A	4B	4C	4D
34		0	1	0	0	4C	4D	4A	4B
35		0	0	1	0	4C	4D	4B	4A
36		0	1	1	0	4A	4B	4D	4C
37		0	0	0	1	4B	4A	4D	4C
38		0	1	0	1	4D	4C	4B	4A
39		0	0	1	1	4D	4C	4D	4C
40		0	1	1	1	4B	4A	4B	4A

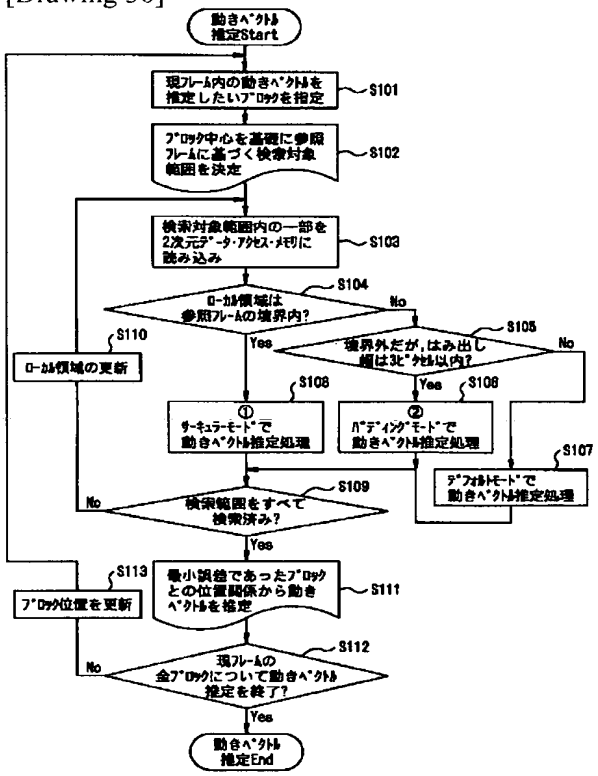
[Drawing 27]

No.	読み出しアクセスモード	読み出しアドレス A0	A1	A4	A5	セレクタ 24A	セレクタ 24B	セレクタ 24C	セレクタ 24D
1	行方向アクセスモード (00)	0	0	0	0	4A	4B	4C	4D
2		1	0	0	0	4B	4C	4D	4A
3		0	1	0	0	4C	4D	4A	4B
4		1	1	0	0	4D	4A	4D	4C
5		0	0	1	0	4C	4D	4A	4B
6		1	0	1	0	4D	4A	4B	4C
7		0	1	1	0	4A	4B	4C	4D
8		1	1	1	0	4B	4C	4D	4A
9		0	0	0	1	4B	4A	4D	4C
10		1	0	0	1	4A	4D	4C	4B
11		0	1	0	1	4D	4C	4B	4A
12		1	1	0	1	4C	4B	4A	4D
13		0	0	1	1	4D	4C	4B	4A
14		1	0	1	1	4C	4B	4A	4D
15		0	1	1	1	4B	4A	4D	4C
16		1	1	1	1	4A	4D	4C	4B
17	列方向アクセスモード (01)	0	0	0	0	4A	4C	4B	4D
18		1	0	0	0	4B	4D	4A	4C
19		0	1	0	0	4C	4A	4D	4B
20		1	1	0	0	4D	4B	4C	4A
21		0	0	1	0	4C	4B	4D	4A
22		1	0	1	0	4D	4A	4C	4D
23		0	1	1	0	4A	4D	4B	4C
24		1	1	1	0	4B	4C	4A	4D
25		0	0	0	1	4B	4D	4A	4C
26		1	0	0	1	4A	4C	4B	4D
27		0	1	0	1	4D	4B	4A	4C
28		1	1	0	1	4C	4A	4D	4B
29		0	0	1	1	4D	4A	4C	4B
30		1	0	1	1	4C	4B	4D	4A
31		0	1	1	1	4B	4C	4A	4D
32		1	1	1	1	4A	4D	4B	4C
33	列方向2段アクセスモード 16bit×2 (10)	0	0	0	0	4A	4B	4C	4D
34		0	1	0	0	4C	4D	4A	4B
35		0	0	1	0	4C	4D	4B	4A
36		0	1	1	0	4A	4B	4D	4C
37		0	0	0	1	4B	4A	4D	4C
38		0	1	0	1	4D	4C	4B	4A
39		0	0	1	1	4D	4C	4A	4B
40		0	1	1	1	4B	4A	4C	4D
41	千鳥モード (11)	0	0	0	0	4A	4C	4B	4D
42		1	0	0	0	4B	4D	4A	4C
43		0	1	1	0	4C	4A	4D	4B
44		1	1	1	0	4D	4B	4C	4A

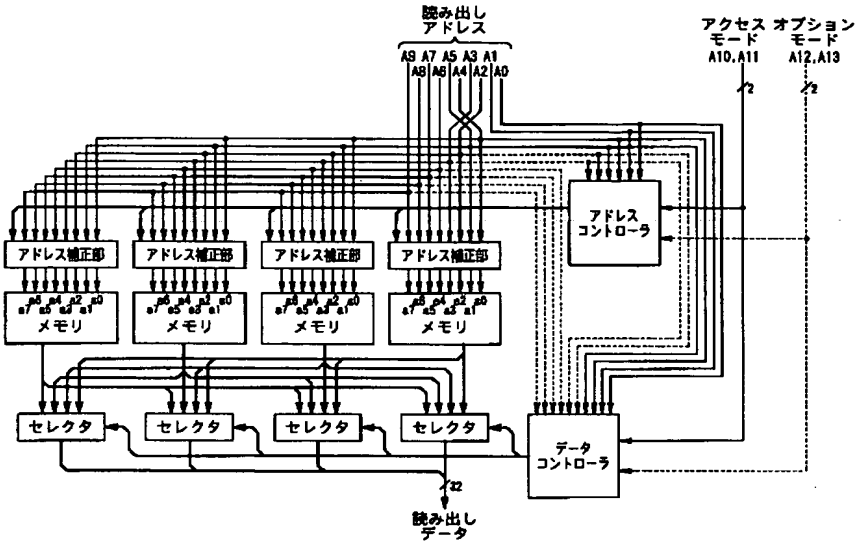
[Drawing 31]



[Drawing 30]



[Drawing 33]



[Translation done.]